Personal Computer
Service Manual

PC-8201

NEC NEC Corporation

PTS-238

CONTENTS

CHAPTER 1
INTRODUCTION

1.1 Specifications

(1) Main Components

a) Keyboard

67 keys	
Function keys:	5
Cursor lead keys:	4
Others:	58

b) LCD

Effective display area:	191.2(W) x 50.4(H) mm
Display panel:	240 x 64 full dot matrix
Dot size:	0.73 x 0.73 mm
Dot pitch:	0.8 mm
Display characters:	40 (characters) x 8 (rows)
Reverse:	By escape sequence

c) Operation Batteries

Batteries:	Four type AA Alkaline-manganese batteries
Operation time:	4.5 days (At four hours/day) 18 days (At one hour/day) **Note:** With I/O disconnected
Battery cassette:	70(W) x 80.5(D) x 19(H) mm
Power OFF:	Manual power off (It is possible to command in BASIC.) (Variable minutes — one to twenty-five minutes)
Low voltage display:	Light a LED (Operate for more than twenty minutes after lighting the LED.)

d) Memory Protection Battery (On main P.C.B)

Battery:	Rechargeable battery
Protection time:	About 26 days (16K bytes) About 7 days (14K bytes)
Recharge method:	Trickle charge by AC adapter or operation batteries

e) LSIs

CPU:	80C85 Code and pin compatible with 8085
ROM:	Standard 32K bytes Option 32K bytes (connect a IC socket)
RAM:	Standard 16K bytes Option 16K bytes (connect a IC socket) Option 32K bytes (connect a IC socket) Option 32K bytes (connect a RAM cartridge)
CLOCK:	2.4 MHz

f) Dimensions:

Front;
300(W) x 215(D) x 35(H) mm
Back:
300(W) x 215(D) x 61(H) mm

(2) I/O interface

a) RS-232C

Word length:	6.7 or 8 bits
Parity:	Non, EVEN or ODD
Stop bit length:	1 or 2 bit
Baud rate:	75, 110, 300, 600, 1200, 2400, 4800, 9600, 19200 BPS

b) SIO2

Distance of transfer:	3 mMin.
Word length:	8 bit
Baud rate:	19200
Parity:	Non
Stop bit:	1 or 2 bit

c) SIO1

Distance of transfer:	3 mMin.
Word length:	8 bits
Baud rate:	19200
Parity:	Non
Stop bit:	1 or 2 bit

d) CMT

Distance of transfer:	1.5 mMin.
Baud rate:	1200 or 600 (switchable by software control)
File format:	Compatible with N-BASIC (binary file only)
Output level:	MIC level

e) Printer: Conforms to Centronics Standards.

f) BCR

g) System slot: For connecting a RAM cartridge.

(3) Special functions: Automatic power OFF
When there is no program operation (awaiting command) for ten minutes, the power is automatically switched off.

1.2 Switches and Contrast VR

(1) POWER Switch
Move this switch towards the rear to turn the power ON. To conserve the batteries, the PC-8201 automatically turns the power off if you do not use it for 10 minutes.
When an automatic power-off occurs, the switch will still be in the ON position even though the power is OFF.
To turn the power ON, move the switch to the OFF position, then back ON.

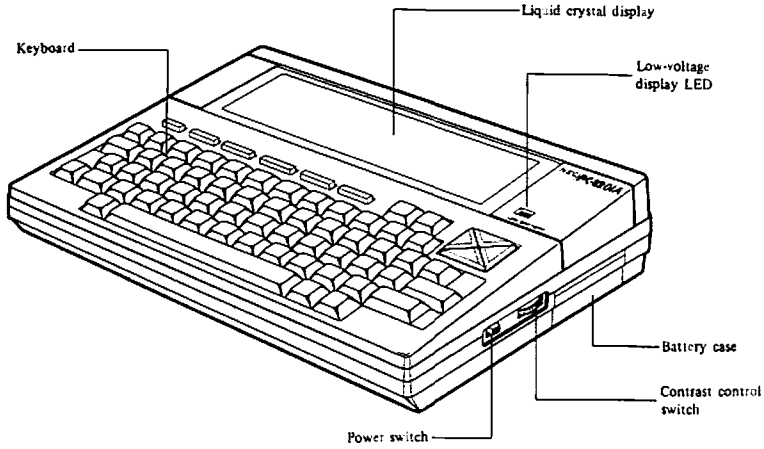
(2) BACK UP POWER Switch
This switch is for preventing discharge of the Ni-Cd battery for RAM back-up.
The PC-8201A will not operate regardless of the setting of the power switch unless this switch is ON. Set this switch to OFF position if the PC-8201 is not to be used for a long time.
Note that the RAM will not be backed up when this switch is set to the OFF position.

(3) RESET Switch
If the PC-8201 "locks-up" (the display will "freeze" and all keys seem to be inoperative), press this button to return to the Main Menu (start-up) screen. It's highly unlikely that the PC-8201 will lock-up when you are using the built-in Application Programs.
However, this situation may occur with customized programs.

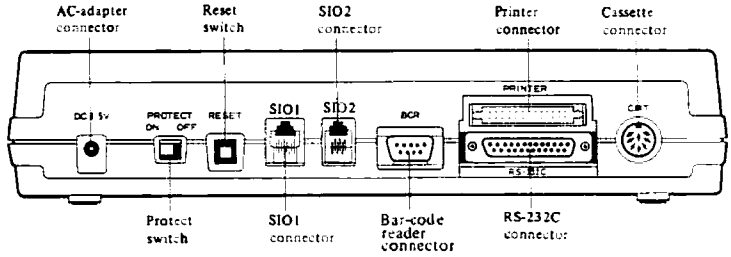
(4) PROTECT Switch
This switch is for protecting the contents of 2nd RAM. (BANK #2)

(5) DISPLAY ADJUSTMENT DIAL
This control is for adjusting the contrast of the LCD display relative to the viewing angle.

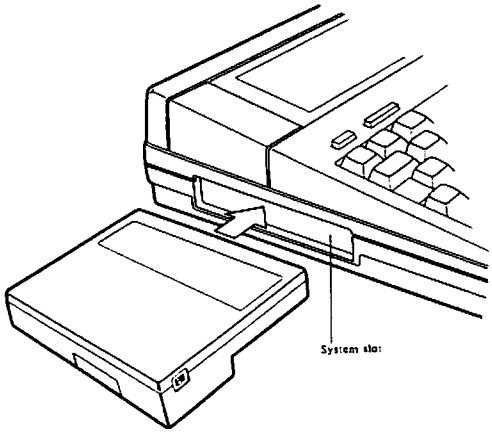
CHAPTER 2
EXTERNAL VIEW



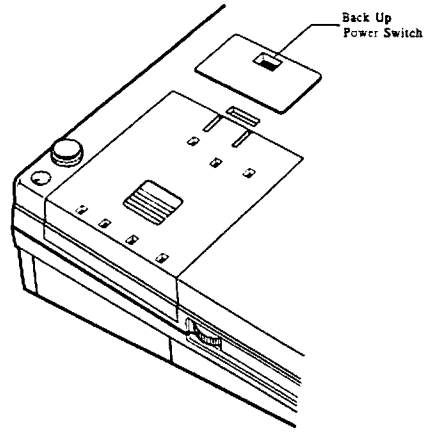
Front



Back



Left Side



Rear View

CHAPTER 3
FUNCTIONAL SPECIFICATIONS

3.1 Logical Specifications

3.1.1 CPU

(1) Available CPU
A 80C85 is used at 2.4 MHz.

(2) How to Reset
There are two kinds of reset: power on reset and manual reset. Pushing the reset switch initiates a warm-start; pushing it while pushing a shift-key and a control-key. initiates a cold-start.

3.1.2 ROM

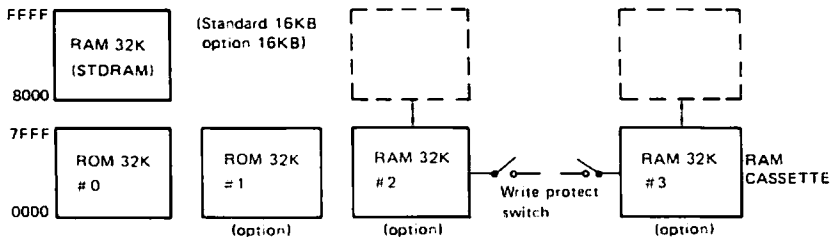
(1) Available ROM
Available ROM is CMOS ROM, and the capacity is 32K byte. (#0)

(2) User ROM
A user ROM is 32K byte. The user ROM area is equipped with an IC socket which can be equipped with CMOS ROM. (#1)

3.1.3 RAM

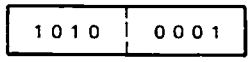
(1) Available RAM
The eight 2K-byte CMOS ICs are used as RAM. The system comes with 16K bytes (STDRAM).

(2) Optional RAM
The PC-8201 is equipped with IC sockets for twenty-four 2K-byte CMOS ICs. 48K bytes. The first 16K bytes of this area are combined with the standard 16K byte RAM to make a 32K byte RAM area. The remaining 32K bytes, become RAM #2. There is also a 32K-byte RAM cassette (#3) port for external memory. It can be connected with a system bus output in PC.

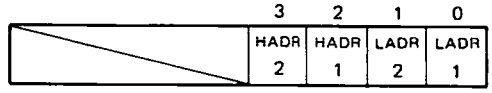


Memory Configuration

Optional RAM #2 and RAM cassette #3 have write protect switches, and they can select the address (0 to 7FFF or 8000 to FFFF) by software control.
Memory is controlled at the following I/O port.



OUT A1H



LADR 2	LADR 1	SELECT ADDRESS (0H to 7FFFH)
0	0	BANK #0 (ROM #0)
0	1	BANK #1 (ROM #1)
1	0	BANK #2 (RAM #2)
1	1	BANK #3 (RAM #3)

HADR 2	HADR 1	SELECT ADDRESS (8000H to FFFFH)
0	0	STANDARD ROM
0	1	NOT USED
1	0	BANK #2 (RAM #2)
1	1	BANK #3 (RAM #2)

3.1.4 LCD Interface

(1) Available driver

HD44102B (Ten)	Segment driver Display RAM 200 byte	
HD44103B (Two)	Common driver	

(2) Available LCD

LR-202C	Number of dots	240 x 64

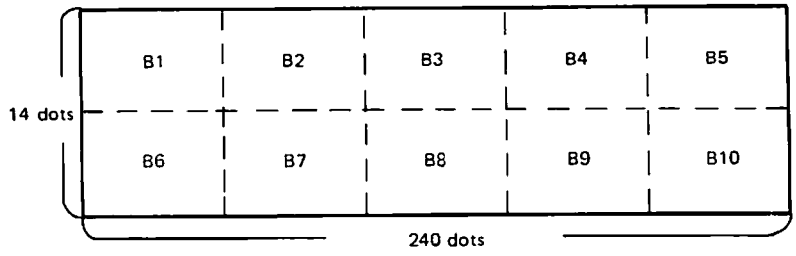
(3) Function of display

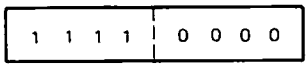
1 Number of display characters
40 characters x 8 rows
(Display duty is 1/32s.)

2 Configuration of character
Both alphanumeric characters and graphic characters can be displayed.

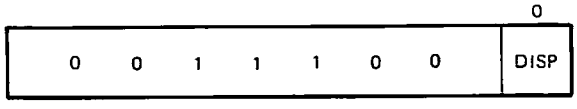
3 LCD I/O address. I/O port
Writing the command to LCD
Reading the status from LCD

* Display On/Off
The LCD is divided into the following IC blocks. Each block can be displayed separately.



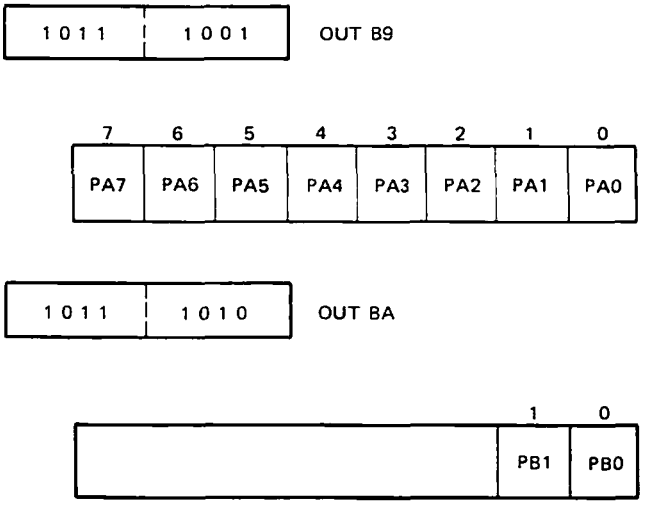


OUT F0



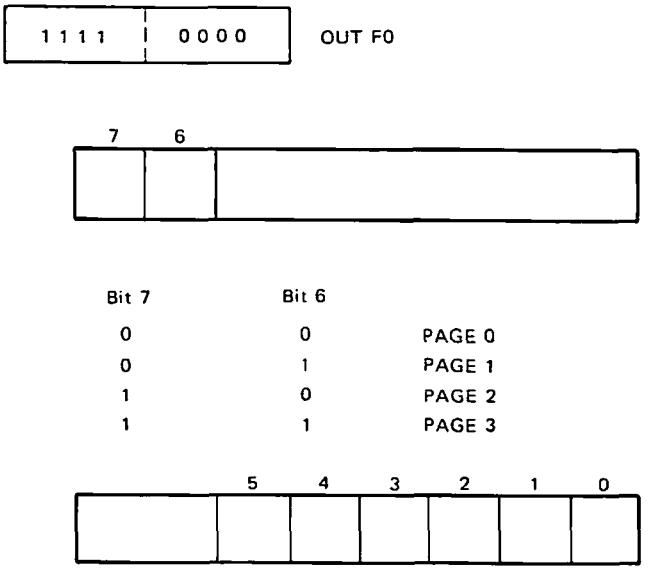
DISP	DISPLAY
0	Off
1	On

The following OUT command selects which block is displayed on or off as Port A and Port B of 81C55.

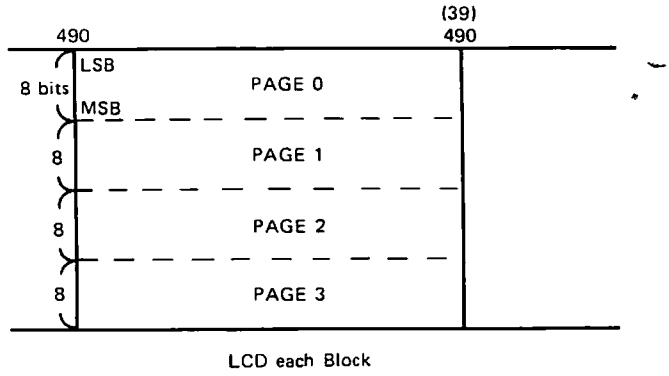


B1 corresponds to PA0, and B2 corresponds to PA1, etc. B10 corresponds to PB1. A1 in each I/O port selects the corresponding LCD block, and is deselected by a 0.

* Address Set



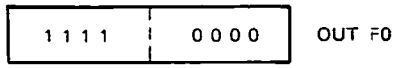
BIT 5 TO BIT 0 0 to 49 displayed by binary number

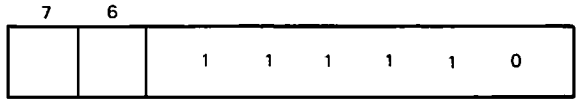


LCD each Block

Set the RAM address in address counter at I/O port (Bit 7 to Bit 0).

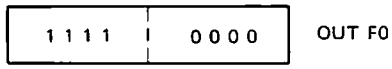
* Set of starting page

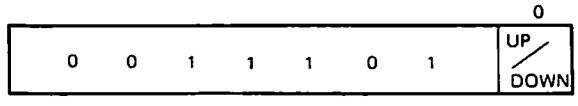




Bit 7	Bit 6		Order of displayed page (One-thityseconds duty)
0	0	:	0, 1, 2, 3
0	1	:	1, 2, 3, 0
1	0	:	2, 3, 1, 0
1	1	:	3, 0, 1, 2

* Select address counter count up or count down

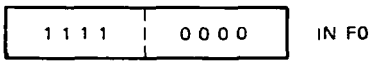


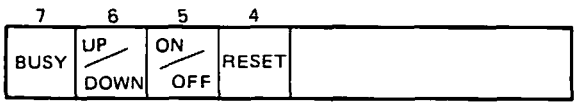


UP/DOWN	SELECT THE ADDRESS COUNTER
0	Down counter
1	Up counter

This address counter is a loop counter whose max is fifty count. After displaying the data, this counter automatically counts up or count down.

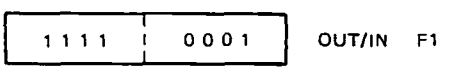
* Read status

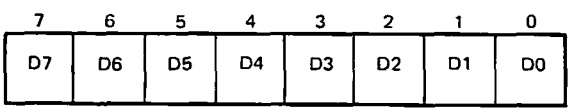




BIT 4	STATE OF RST PIN
0	Normal
1	RST is low level, BUSY in Bit 7 is 1.
BIT 5	DISPLAY ON/OFF
0	Display Off
1	Display On
BIT 6	TYPE OF ADDRESS COUNTER
0	Down counter
1	Up counter
BIT 7	OPERATE THE COMMAND
0	Normal
1	Operate IN F1, OUT F0, and OUT F1 command

* Write or Read Display Data





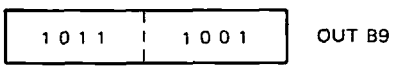
BIT 7~ BIT 0 Displayed data

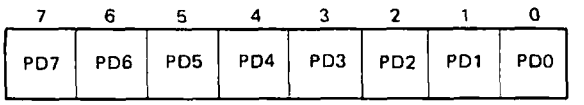
This operates access with the RAM whose address has already been selected. After then, the address counter is counted up or counted down.

3.1.5 Printer Interface

The printer interface is an 8-bit parallel interface (Centronics compatible). The following shows the printer interface port. Data is transmitted to Port A at 81C55, and control signal from printer is transmitted to Port C.

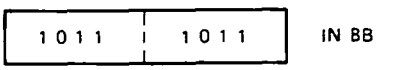
* Data transfer to printer

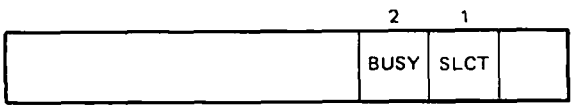




BIT 7 ~ BIT 0 Printer data port

* BUSY, SLCT signal from printer





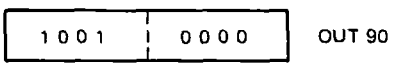
SLCT

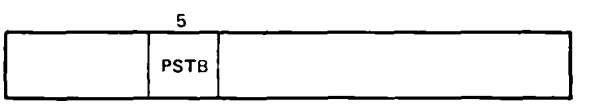
0	Deselect
1	Select

BUSY

0	Printer READY
1	Printer BUSY

* Strobe printer



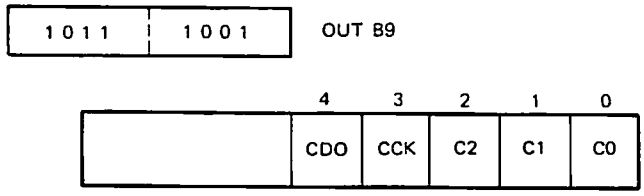


PSTB	STROBE PRINTER
0	Strobe Off
1	Strobe On

3.1.6 Calendar Clock Interface

Calendar clock interface is equipped with an LSI for watch (μPD1990AC). The following shows the I/O port.

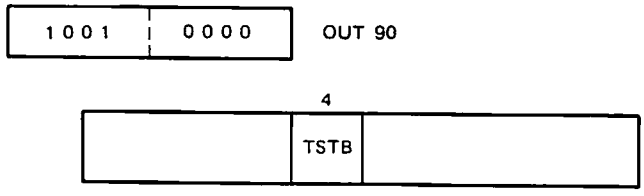
* Command data output port



C2, C1, C0	Command output port
CCK	SHIFT CLOCK
0	Clock Off
1	Clock On
CDO	Data output port

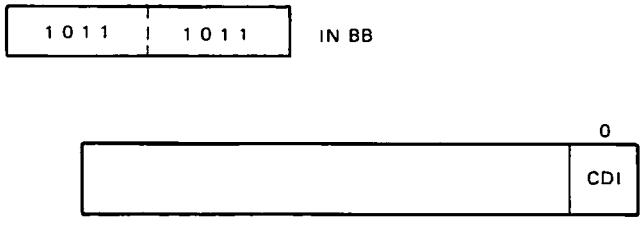
The first value is 05H

* Command Strobe to the Clock



TSTB	COMMAND STROBE TO CLOCK
0	Strobe Off
1	Strobe On

* Data from Clock



CDI	CLOCK DATA INPUT PORT

3.1.7 Keyboard Interface

The keyboard is sensed by a software scan. It transmits low signals (OUT B9, OUT BA) to Port A or Port B at 81C55, and senses the depressed key by IN E8.

* Keyboard Interface Port

1011	1001

OUT B9

PA7 ~ PA0	Key
00000001	L ~ Z
00000010	K ~ A
00000100	I ~ Q
00001000	^] ~ O
00010000	8 (~ 1 !
00100000	PAST INS ~ 9)
01000000	@ ~ DEL BS
10000000	STOP ~ f

1011	1010

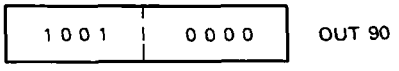
OUT BA

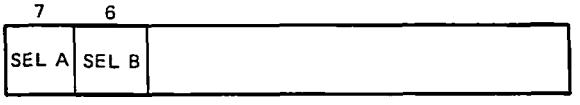
PB7 ~ PB0	Key
00000001	CAPS ~ SHIFT

3.1.8 Serial Interface

The serial interface uses an RS-232C, SIO1, or SIO2, switching them one another, by USART IM6402.

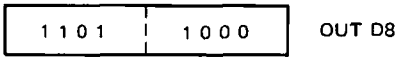
* Interface Switching

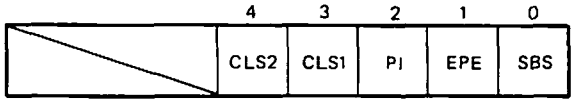




SEL A	SEL B	
0	0	NOT USED
0	1	SIO2
1	0	SIO1
1	1	RS-232C

* Load to USART and control register





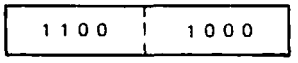
SBS	
	STOP BIT SELECT
0	Stop bit length 1 bit
1	If the length of data is 5 bits, it is 5 bits. In other cases, it is 1.5 bits

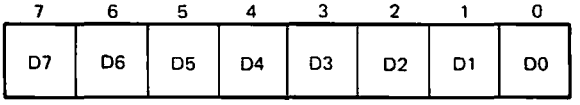
EPE	
	ODD PARITY/EVEN PARITY
0	Odd parity
1	Even parity

PI	
	DISPLAY PARITY
0	Parity generation check
1	Disable parity generation check

CLS 2	CLS 1	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

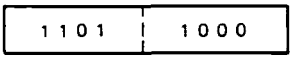
* USART I/O data

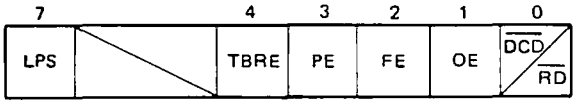




D7 ~ D0 USART DATA PORT

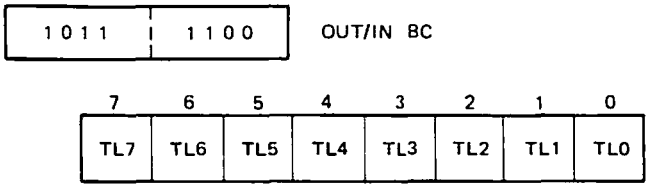
* USART Status Read



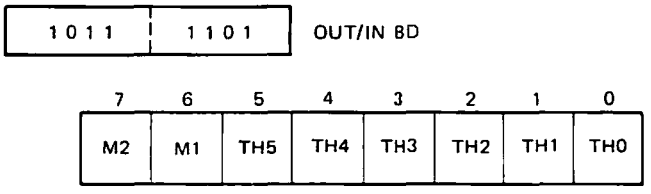


$\overline{DCD}/\overline{RD}$	DATA CARRIER DETECT/RING DETECT
0	On
1	Off
OE	OVERRUN ERROR
1	Generate an overrun error
FE	FRAMING ERROR
1	Generate a framing error
PE	PARITY ERROR
1	Generate a parity error
TBLE	TRANSMITTER BUFFER REGISTER EMPTY
1	Able to transmit data
LPS	LOW POWER SIGNAL
1	Dropped Power Voltage

* 81C55 Timer control for establishing UART Baud Rate



TL7 ~ TL0 Timer Counter Lower 8-bit



TH5 ~ TH0 Timer Counter Upper 6-bit

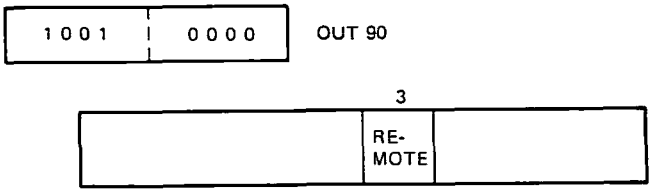
M2	M1	
0	0	This mode transmits a single-square wave which the first half of the number of count is high and remaining is low. (Mode 0)
0	1	This mode continually transmits a Mode 0 type square wave. (Mode 1)
1	0	This mode transmits an L-pulse (single pulse) during one clock when finishing the terminal count. (Mode 2)
1	1	This mode continually transmits a Mode 2 type pulse. (Mode 3)

The OUT BD command loads the time constant to the time constant register (Bit 0 to Bit 13), and also loads the mode of timer to bit 14 and bit 15.
The IN BD command reads the contents of the counter (count data) and the mode bit.

3.1.9 Cassette Interface

The cassette interface uses SID (Serial Input Data) and SOD (Serial Output Data) at 80C85.

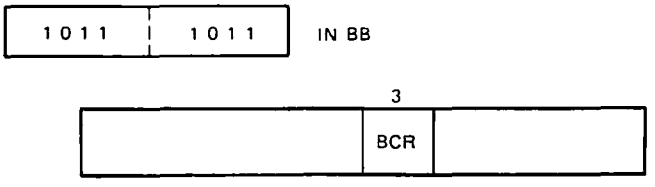
* Cassette Motor control



REMOTE	MOTOR CONTROL
0	Motor Off
1	Motor On

3.1.10 Bar Code Reader Interface

* Data from bar code reader



BCR	Data from Bar Code Reader

3.1.11 Interrupt Functions

The PC-8201 is equipped with a 4-priority level interrupt control logic. The interrupts are input to the 80C85 (TRAP, RST 7.5, 6.5, 5.5). TRAP is nonmaskable; the others can be masked by software control.

Priority	Interrupt Channel	Function
High	TRAP	POWER TRAP
↓	RST 7.5	KEY INT
↓	RST 6.5	UART
Low	RST 5.5	BCR

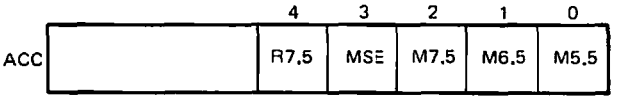
POWER TRAP — Power voltage is low. If it becomes less than a certain value, the interrupt is enabled and power automatically turns off.

KEY INT — Searches the input key by the 256 kHz clock which is transmitted from the timer chip, μPD1990AC.

UART — Received interrupt from UART IM6402

BCR — Interrupt from bar code reader

All interrupts except TRAP have an exclusive use mask flag, so each can be individually masked. The mask flag is set or reset by the SIM (Set Interrupt Mask) command.

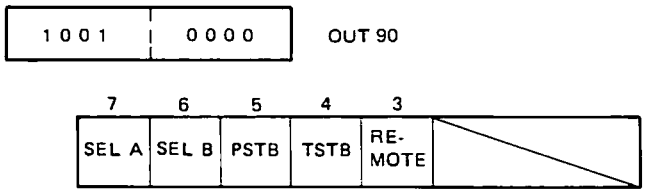


See the command of 80C85.

3.1.12 I/O Address

UPPER I/O ADDRESS MSB	FUNCTION
1 0 0 0	ROM Cassette
1 0 0 1	System Control Port
1 0 1 0	Bank Control Port
1 0 1 1	PIO 81C55 Port
1 1 0 0	UART DATA Port
1 1 0 1	UART Control Port
1 1 1 0	Keyboard
1 1 1 1	LCD

(1) System Control



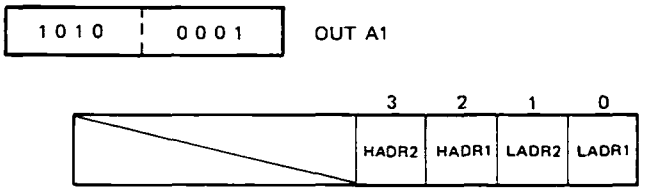
REMOTE	CASSETTE MOTOR CONTROL
0	Motor Off
1	Motor On

TSTB	CLOCK COMMAND STROBE
0	Strobe Off
1	Strobe On

PSTB	PRINTER STROBE
0	Strobe Off
1	Strobe On

SEL A	SEL B	SERIAL INTERFACE SELECT
0	0	Not Used
0	1	SIO2
1	0	SIO1
1	1	RS-232C

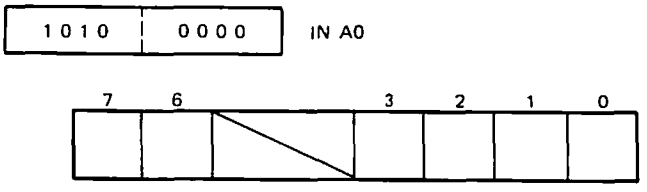
(2) Bank Control



LADR 2	LADR 1	SELECT ADDRESS 0H TO 7FFFH
0	0	Bank #0 (ROM #0)
0	1	Bank #1 (ROM #1)
1	0	Bank #2 (RAM #2)
1	1	Bank #3 (RAM #3)

HADR 2	HADR 1	SELECT ADDRESS 8000H to FFFFH
0	0	Standard RAM
0	1	Not Used
1	0	Bank #2 (RAM #2)
1	1	Bank #3 (RAM #3)

(3) Bank Status



BIT 1	BIT 0	STATUS OF 0H TO 7FFFH
0	0	Bank #0 (ROM #0)
0	1	Bank #1 (ROM #1)
1	0	Bank #2 (RAM #2)
1	1	Bank #3 (RAM #3)

BIT 3	BIT 2	STATUS OF ADDRESS 8000H TO FFFFH
0	0	Standard RAM
0	1	Not Used
1	0	Bank #2 (RAM #2)
1	1	Bank #3 (RAM #3)

BIT 7	BIT 6	STATUS OF SERIAL INTERFACE
0	0	Not Used
0	1	SIO2
1	0	SIO1
1	1	RS-232C

(4) PIO 81C55 Address

I/O Address		Select
1011	1000	Internal command/Status register
	1001	General I/O Port A (PA0 to PA7)
	1010	General I/O Port B (PB0 to PB7)
	1011	General I/O Port C (PC0 to PC5)

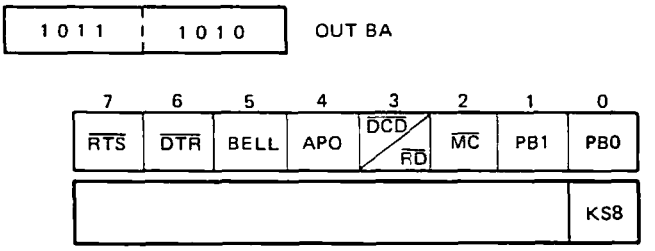
* Port A output

1011	1001	OUT B9

7	6	5	4	3	2	1	0
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
KS7	KS6	KS5	KS4	KS3	KS2	KS1	KS0
			CCK	CD0	C2	C1	C0

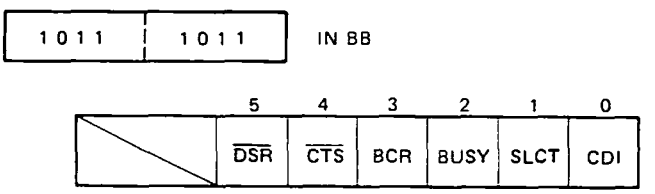
PA7 to PA0	LCD Chip Select
PD7 to PD0	Printer Data Port
KS7 to KS0	Keyboard
C2 to C0	Clock Command Output Port
CDO	Clock Data Output Port
CCK	Calendar Shift Clock
0	Clock Off
1	Clock On

* Port B Output



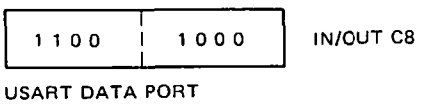
PB1 ~ PB0	LCD Chip Select
$\overline{MC}$	MELODY CONTROL OUTPUT
0	On
1	Off
DCD/$\overline{RD}$	DCD/RD SELECT OF THE RS-232C
0	Ring Detect
1	Data Carrier Detect
APO	AUTO POWER OFF OUTPUT
0	Output Off
1	Output On
BELL	BUZZER OUTPUT
0	Ring
1	Not Ring
$\overline{DTR}$	RS-232C DTR output Active Low
$\overline{RTS}$	RTS output Active Low

* Port C Input



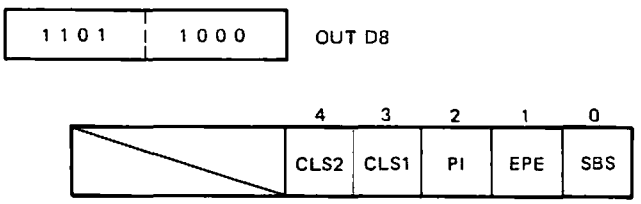
CDI	Clock Data Input Port
SLCT	PRINTER BUSY
0	Printer Ready
1	Printer Busy
BCR	Bar Code Reader Data Input Port
$\overline{CTS}$	CTS Input Active Low
$\overline{DSR}$	RS-232C DSR Input Active Low

(6) USART Data I/O Port



(7) Usart Control Port

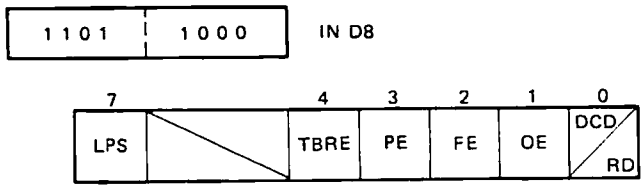
* Command Write



SBS	STOP BIT SELECT
0	Stop bit length is 1 bit.
1	If data length is 5 bits, stop bit length is 1.5 bits. In the other case, it is 2 bit.
EPE	EVEN PARITY ENABLE
0	Odd Parity
1	Even Parity
PI	PARITY INHIBIT
0	Generate parity and check
1	Inhibit generating parity and check

CLS2	CLS1	CALENDAR LENGTH SELECT
0	0	Data Length 5 bits
0	1	Data Length 6 bits
1	0	Data Length 7 bits
1	1	Data Length 8 bits

* Status read



DCD/RD	
0	On
1	Off

OE	Overrun Error
1	Detected

FE	Framing Error
1	Detected

PE	Parity Error
1	Detected

TBRE	Transmitter Buffer-register Empty
1	ready to receive data to transmit

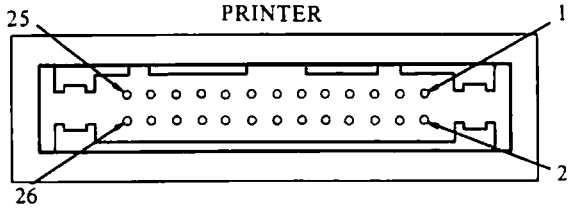
LPS	LOW POWER SIGNAL
1	low power voltage

3.2 Physical Specifications

3.2.1 Signal Lines

(1) Printer Interface

· Printer 26 pin connector using a flat cable

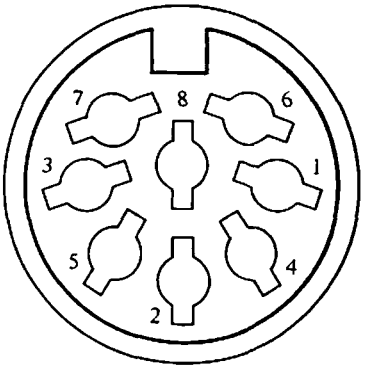


Pin number	Signal name	Remarks	Pin number	Signal name	Remarks
1	STROBE	Write strobe	2	GND	Signal ground
3	PD0	Parallel data 0	4	GND	Signal ground
5	PD1	Parallel data 1	6	GND	Signal ground
7	PD2	Parallel data 2	8	GND	Signal ground
9	PD3	Parallel data 3	10	GND	Signal ground
11	PD4	Parallel data 4	12	GND	Signal ground
13	PD5	Parallel data 5	14	GND	Signal ground
15	PD6	Parallel data 6	16	GND	Signal ground
17	PD7	Parallel data 7	18	GND	Signal ground
19	NC		20	GND	Signal ground
21	BUSY	Printer busy	22	GND	Signal ground
23	NC		24	GND	Signal ground
25	SLCT	Printer select	26	NC	

(2) CMT Interface

· CMT 8-pin DIN CONNECTOR

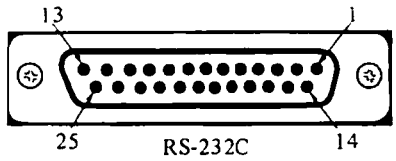
CMT



Pin number	Signal name	Remarks
1	T x C	TTL level output
2	GND	Signal ground
3	GND	Electrical power ground
4	MIC	Output to MIC
5	EAR	Input from EAR
6	REM1	Remote terminal
7	REM2	Remote terminal
8	Vcc	+5 V

(3) RS-232C Interface

· RS-232C 25-pin D SUB CONNECTOR

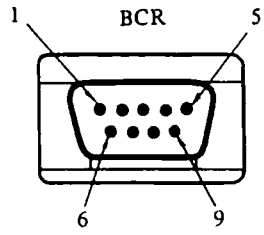


Pin number	Signal name	Remarks
1	GND	Protective ground
2	TxD	Transmit data
3	RxD	Receive data
4	RTS	Request to send
5	CTS	Transmission authorized
6	DSR	Data set relay
7	GND	Signal ground
8	DCD	Data carrier detect
≀		
20	DTR	Data carrier ready
22	RD	Bell detect
25	---	

Either 8-pin (DCD) or 22-pin (RD) can be selected by software control.

(4) Bar Code Reader Interface

· BCR 9-pin D SUB CONNECTOR

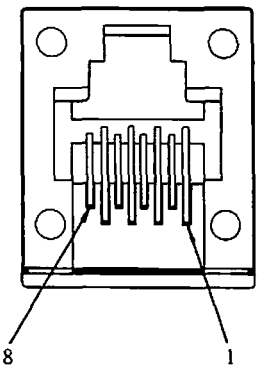


Pin number	Signal name	Remarks
1	NC	Not connected
2	R x DB	Receive data
3	NC	Not connected
4	NC	Not connected
5	GND	Signal ground
6	NC	Not connected
7	GND	Signal ground
8	NC	Not connected
9	Vcc	+5 V

(5) SIO1 Interface

· SIO1 8-pin DuPont BERG modular jack

SIO1

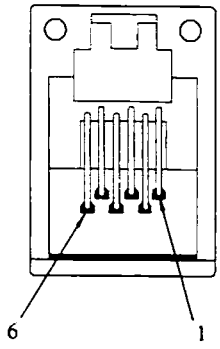


Pin number	Signal name	Remarks
1	GND	Signal ground
2	TxD	Transmit data
3	RxR	Receive data
4	RTS	Request to send
5	CTS	Transmission authorized
6	Vcc	+5 V
7	NC	Not connected
8	NC	Not connected

(6) SIO2 Interface

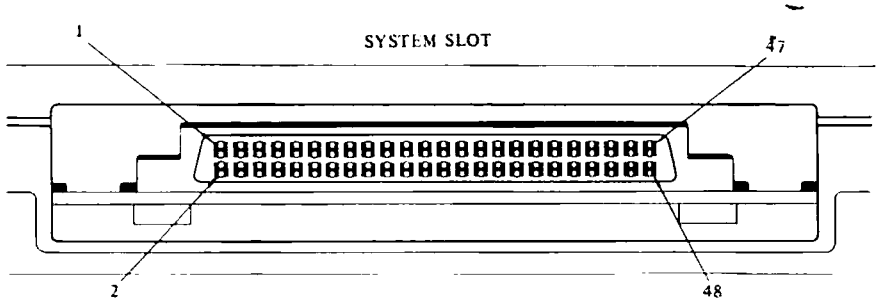
· SIO2 6-pin DuPont BERG modular jack

SIO2



Pin number	Signal name	Remarks
1	GND	Signal ground
2	TxD	Transmit data
3	RxR	Receive data
4	RTS	Request to send
5	CTS	Transmission authorized
6	Vcc	+5 V

(7) ROM Cassette/System Bus



Pin number	Signal name	Remarks
1	VDD	+5 V
2	VDD	+5 V
3	AD0	Address/Data 0
4	AD4	Address/Data 4
5	AD1	Address/Data 1
6	AD5	Address/Data 5
7	AD2	Address/Data 2
8	AD6	Address/Data 6
9	AD3	Address/Data 3
10	AD7	Address/Data 7
11	NC	No Connection
12	NC	No Connection
13	A8	Address 8
14	A12	Address 12
15	A9	Address 9
16	A13	Address 13
17	A10	Address 10
18	A14	Address 14

(Cont)

Pin number	Signal name	Remarks
19	A11	Address 11
20	A15	Address 15
21	A16	Address 16
22	A18	Address 18
23	A17	Address 17
24	A19	Address 19
25	NC	No Connection
26	NC	No Connection
27	$\overline{RD}$	Read
28	$\overline{WR}$	Write
29	IO/M	IO OR Memory
30	ALE	Address Latch Enable
31	HOLD	HOLD
32	HOLDA	HOLD Acknowledge
33	INTR	INTERRUPT
34	$\overline{INTA}$	INTER Acknowledge
35	RESET	RESET
36	READY	READY
37	ROME	ROM Enable
38	E	Enable
39	BANK#3	ROM Cassette Select signal
40	NC	No Connection
41	HADRD	High Address Disable
42	LADRD	Low Address Disable

(Cont)

Pin number	Signal name	Remarks
43	CLK	Clock
44	POWER	RAM Protect signal
45	GND	Ground
46	GND	Ground
47	NC	No Connection
48	NC	No Connection

3.2.2 Power Supply

The PC-8201 can operate with the three types of power supply.

(1) SUM-3 dry cells (Four)
AM-3 (Alkali Manganese dry cell)
This can be used for more than 18 hours.
(Normal: at standby: 16K RAM)

SM-3 (Manganese dry cell)
This can be used for more than 6 hours.
(Normal: at standby: 16K RAM)

(2) Ni-Cd battery PC-8201-90
This can be used for more than 5.5 hours.
(Normal temperature: at standby: 16K RAM)
It is possible to floating charge.
charge 48 H
No time limit for recharging
It is charged in spite of power on or off of the PC-8201.

(3) AC adapter PC-8271-01

The AC adapter specifications are based on the functional specifications of the PC-8271-01. The PC-8201 has an EMERGENCY battery.

Backup time:

System equipped with 64K	More than 7 days (Normal)
System equipped with 16K	More than 26 days (Normal)

Battery is changed by AC adapter or operation battery.
A backup power switch can disable to backup or floating charge.

3.2.3 Structure and Size

The mechanism is shown in appendix, also the color, the display characters, and the case style are shown in it.

3.3 Interface to Other Hardware

(1) RS-232C
This port is compatible with the RS-232C standard.

(2) Printer
Can be directly connected with printers with Centronics compatible port.

(3) Bar Code Reader
Can be directly connectes with a bar code reader with a Centronics compatible parallel port.

(4) Audio Cassette Tape Recorder
Can be directly connected with commercial audio cassette tape recorder.

(5) Serial I/O
Can be directly connected with peripheral interfaces having a CMOS serial interface.

(6) ROM/RAM Cartridge
Use to expand the system bus slot.

(7) Other Peripheral Circuits
Via system bus slot

3.4 Software Interface

The PC-8201 is a peripheral computer which uses 8-bit CMOS and an 80C85 CPU. The command set is the same as the 8085.

3.5 Human Interface

(1) LCD display
A 240 x 64 dot full graphic LCD display is used. The standard display character is 40 characters x 8 rows.

It is possible to control the contrast by volume. The contrast is changed by view angle.

(2) Keyboard

The following show the key arrangement of keyboard unit and a table of character codes. The F-key and J-key, which is key tops of home position, have tubarcles. The key tops are made from standard plates made by Alps.

1 PC-8201 Keyboard

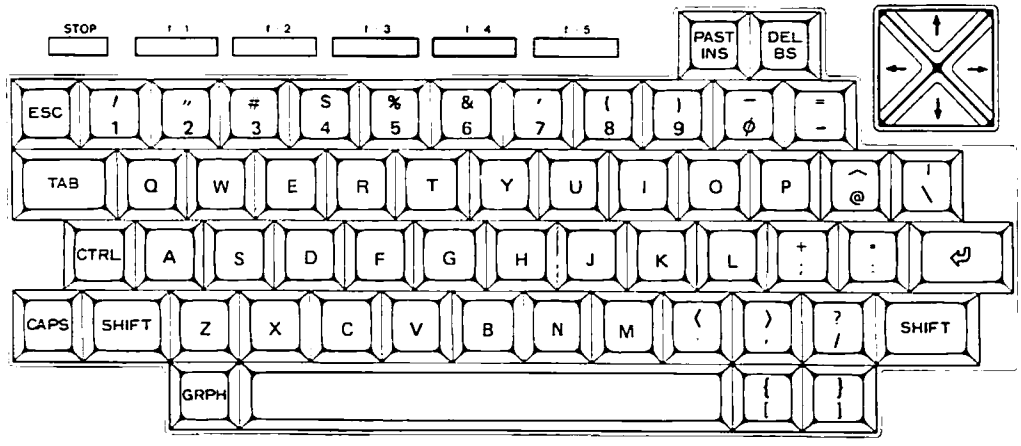
Character codes 60H and 7EH cannot be transmitted from the keyboard.

2 Graphic key combination input

Character codes 80H to 9FH can be input by depressing key together with the graphic key. Character codes A0H to BFH can be input by combining the graphic key and shift key.

3 User Defined Characters

Character codes 83H to FFH can be defined by the user.



PC-8201 Key Arrangement

PC-8201 Character Code

H / L	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111
0 0000	C/@	C/P	SPACE	0	@	P	`	p	G/Z ◀	G/Q	GS/Z	GS/Q				
1 0001	C/A SHIFT→	C/Q C/←	!	/	A	Q	a	q	G/X ↵	G/W	GS/X	GS/W				
2 0010	C/B SHIFT/↑	C/R INS C/→	"	2	B	R	b	r	G/C ▩	G/E	GS/C	GS/E				
3 0011	C/C STOP	C/S	#	3	C	S	c	s	G/V	G/R	GS/V	GS/R				
4 0100	C/D	C/T SHIFT/↑	$	4	D	T	d	t	G/B	G/T	GS/B	GS/T				
5 0101	C/E	C/U	%	5	E	U	e	u	G/N	G/Y	GS/N	GS/Y				
6 0110	C/F SHIFT→	C/V	&	6	F	V	f	v	G/M	G/U	GS/M	GS/U				
7 0111	C/G	C/W C/↑	'	7	G	W	g	w	G/L	G/I	GS/L	GS/I				
8 1000	C/H BS	C/X	(	8	H	X	h	x	G/A	G/O	GS/A	GS/O				
9 1001	C/I	C/Y	)	9	I	Y	i	y	G/S	G/P	GS/S	GS/P				
A 1010	C/J	C/Z C/↓	*	:	J	Z	j	z	G/D	G/@	GS/D	GS/\				
B 1011	C/K	ESC	+	;	K	[	k	{	G/F	G/\	GS/F	GS/:				
C 1100	C/L	→	,	<	L	\	l	|	G/G	G/,	GS/G	GS/<				
D 1101	C/M ↵	←	-	=	M	]	m	}	G/H	G/.	GS/H	GS/>				
E 1110	C/N	↑	.	>	N	^	n	~	G/J	G/	GS/J	GS/?				
F 1111	C/O	↓	/	?	O	_	o	(DEL)	G/K	G/]	GS/K	GS/}				

Notes: C/ means CTRL +.
G/ means GRPH +.
GS/ means GRPH + SHIFT +.

3.6 Performance Specification for the PC-8201

CPU	80C85 2.4 MHz operation
ROM	32K bytes (Max 64K bytes)
RAM	16K bytes (Max 64K bytes)
LCD display	240 x 64 dots (40 characters x 8 rows)
Printer I/F	Centronics specification; one channel
Calendar watch	D1990AC
Keyboard	Keyboard (See Item 4.5.)
Serial I/F	300 to 19200 baud CMOS level two connectors
RS-232C I/F	300 to 19200 baud 5 V output one channel (Serial I/F uses the same serial channel as the RS-232C I/F by switching.)
CMT I/F	Compatible with the PC-8001
Bar Code Reader	Based on HREDS-3050 interface made by Hewlett-Packard.

3.7 Accessories

(1)	CMT cable	1
(2)	Demo tape	1
(3)	Soft case	1
(4)	Users manual	1
(5)	Reference manual	1
(6)	Warranty	1

CHAPTER 4
DISASSEMBLY/REASSEMBLY

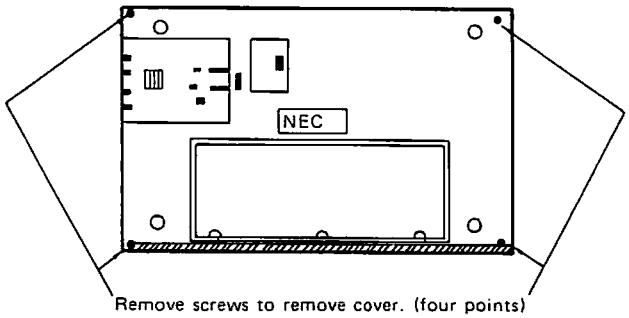
4.1 Disassembly

* Save any data caution in the RAM before continuing.

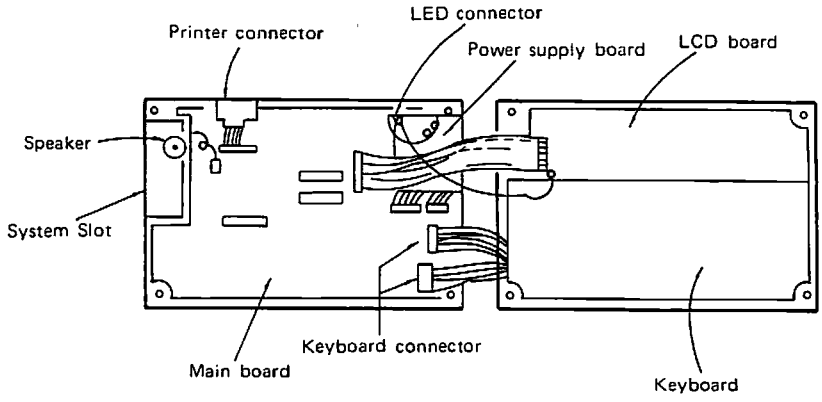
* Turn off the PC-8201 power. Remove the battery case, turn off the backup power switch. (If using an AC adapter, remove it also.)

4.1.1 PC-8201 Cover

Bottom Side

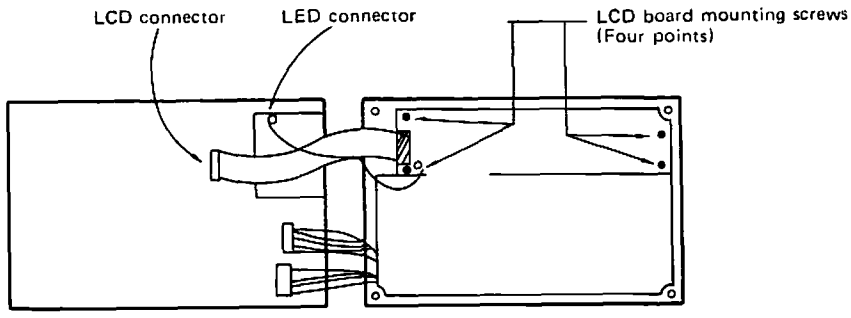


Turn the PC-8201 over, and unscrew. (eleven points)



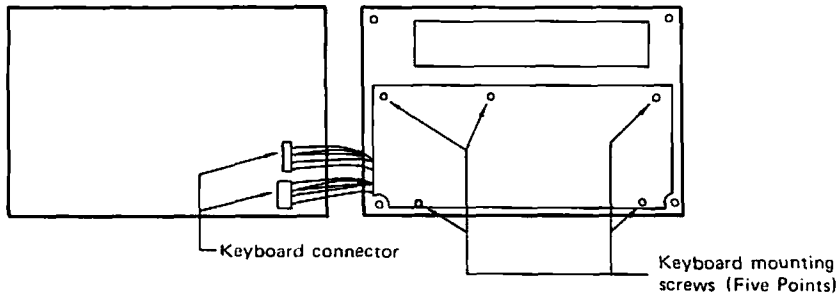
Uncovered PC-8201

4.1.2 LCD Board



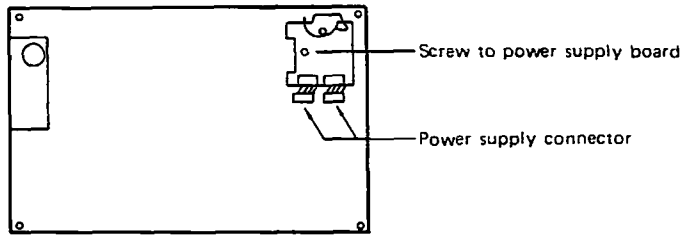
Remove LCD connector and LED connector; unscrew LCD board. (Four points)

4.1.3 Keyboard



Remove the two keyboard connectors; unscrew the keyboard. (Five Points)

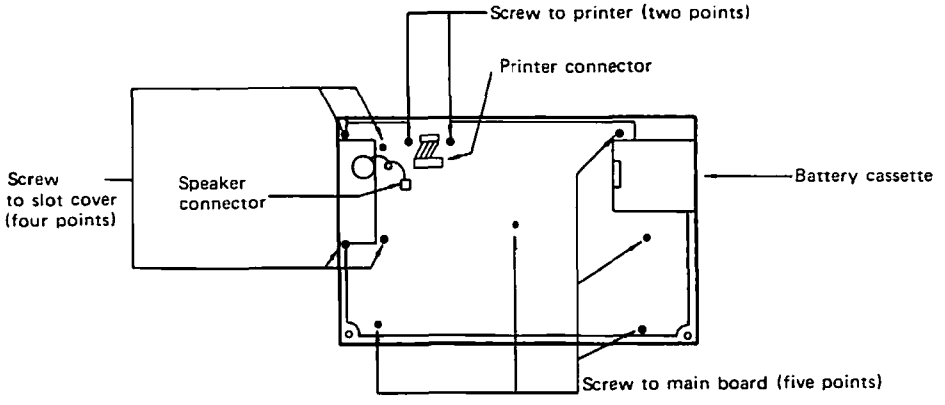
4.1.4 Power Supply Board



Remove power supply connector; unscrew the power supply board.

4.1.5 Main Board

* Remove the battery cassette before continuing.



If removing the main board, unscrew the followings.

* Printer connector (Two)
* Speaker connector
* Slot cover (Four)
* Main board (Five)

4.2 Reassembly

CAUTION

Before continuing, save any data in RAM using the cassette tape. After completing adjustments, reload RAM from the cassette.

4.2.1 LCD Board

(1) Turn off the power; remove the battery case: turn off the backup power switch. (If using an AC adapter, remove it also.)

(2) Remove the PC-8201 cover
Remove the LCD board

(3) Replace the LCD board

(4) To reassemble, follow these steps in reverse.

4.2.2 Keyboard

(1) Turn off the power; remove the battery case; turn off the backup power switch. (If using an AC adapter, remove it also.)

(2) Remove the PC-8201 cover.
Remove the keyboard.

(3) Replace the keyboard.

(4) To reassemble, follow these steps in reverse.

4.2.3 Keyboard Switch

(1) Turn off the power; remove the battery case; turn off the backup power switch. (If using an AC adapter, remove it also.)

(2) Remove the PC-8201 cover.
Remove the keyboard switch.

(3) Search for the key number of the keyboard switch to be changed. The key number is written on the keyboard printed circuit board.

(4) Remove the solder from the key switch to be changed. (When removing solder, be careful not to damage or cut the pattern.)

(5) Pull out the key top.

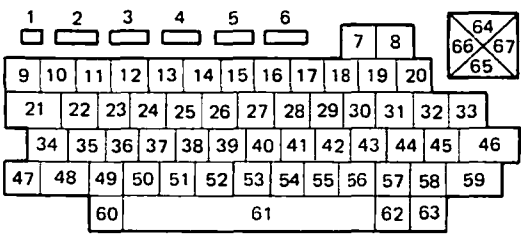
(6) Remove the key switch. (Pull up, pinching the lock with pliers.)

(7) When installing a new switch, press it down until it comes into contact with the base plate.

(8) Solder the new key switch to the keyboard printed circuit board.

(9) Insert the key top.

(10) Reassemble in reverse order.



Key Number

4.2.4 Power Supply Board

(1) Turn off the power; remove the battery case; turn off the backup power switch. (If using an AC adapter, remove it also.)

(2) Remove PC-8201 cover.
Remove power supply connector.
Remove power supply board.

(3) Replace power supply board.

(4) Reassemble in reverse order.

4.2.5 Main Board

(1) Turn off the power; remove the battery case; turn off the backup power switch. (If using an AC adapter, remove it also.)

(2) Remove PC-8201 cover.
Remove LCD connector.
Remove LED connector.
Remove keyboard connector.
Remove power supply connector.
Remove main board.

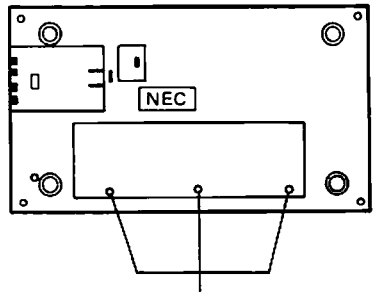
(3) Replace the main board.

(4) Reassemble in reverse order.

4.2.6 ROM

(1) Turn off the power; remove the battery case; turn off the backup power switch. (If using an AC adapter, remove it also.)

(2) Unscrew the ROM cover. (Three points)



ROM Cover Screws

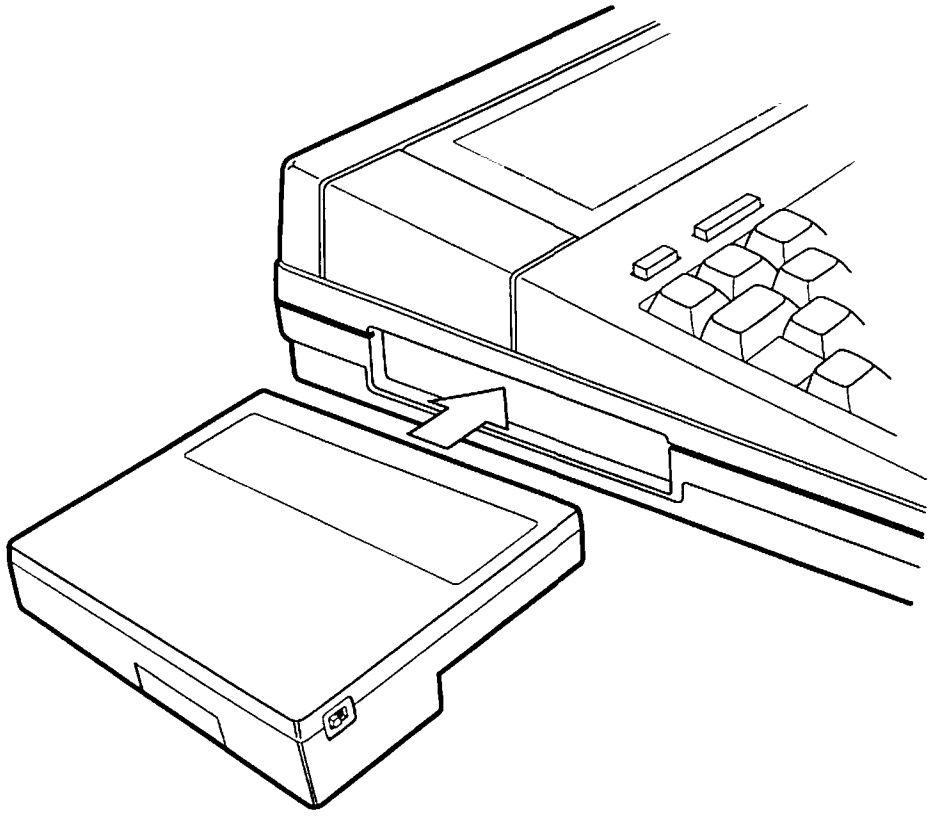
(3) Remove the two old ROM chips. (Use a screwdriver between the socket and the ROM and gently pry up.)

(4) Insert new ROM chips in socket.

(5) Replace ROM cover.

4.3 Installation

4.3.1 Inserting Cartridge (RAM, ROM)



Left Side

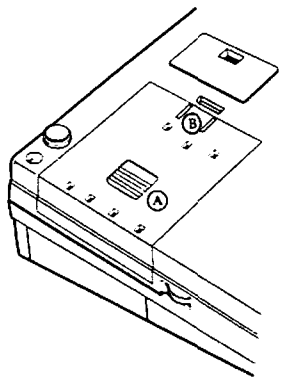
– System Slot –
When using RAM cartridge or ROM cartridge. insert into the system slot.

* If inserting the cartridge, turn off the power and insert cartridge firmly.

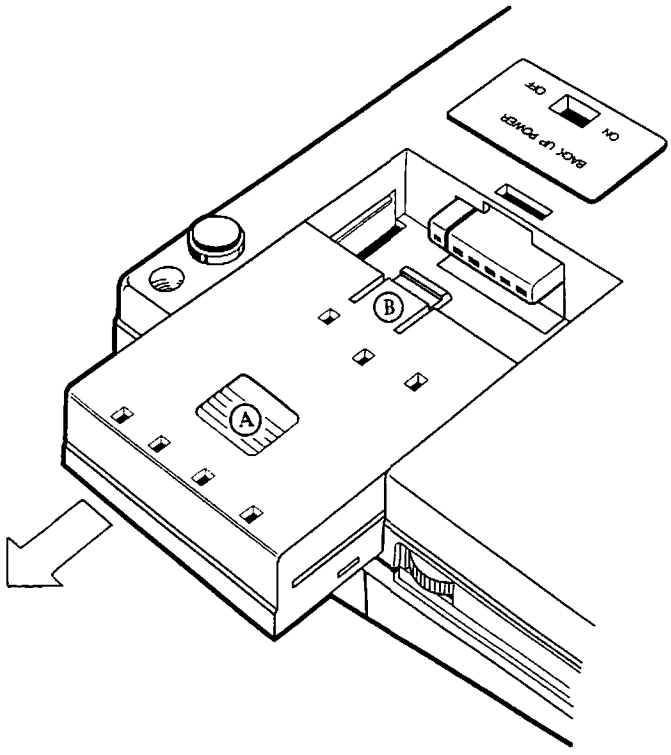
4.3.2 Battery Installation

The PC-8201 is operated by four SUM-3 batteries. The PC-8201 is not shipped with batteries inserted. The following procedure explains how to insert.

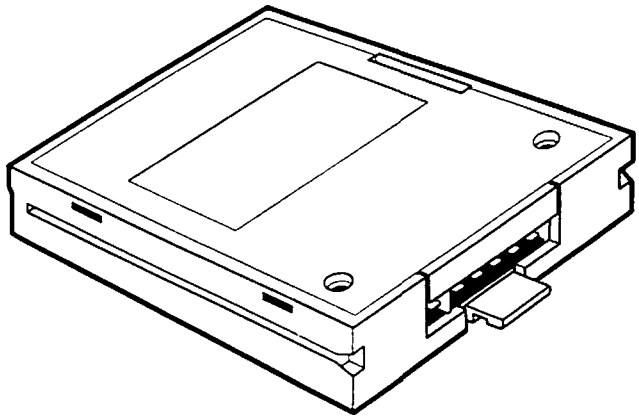
(1) Turn off the power, and turn unit upside down.



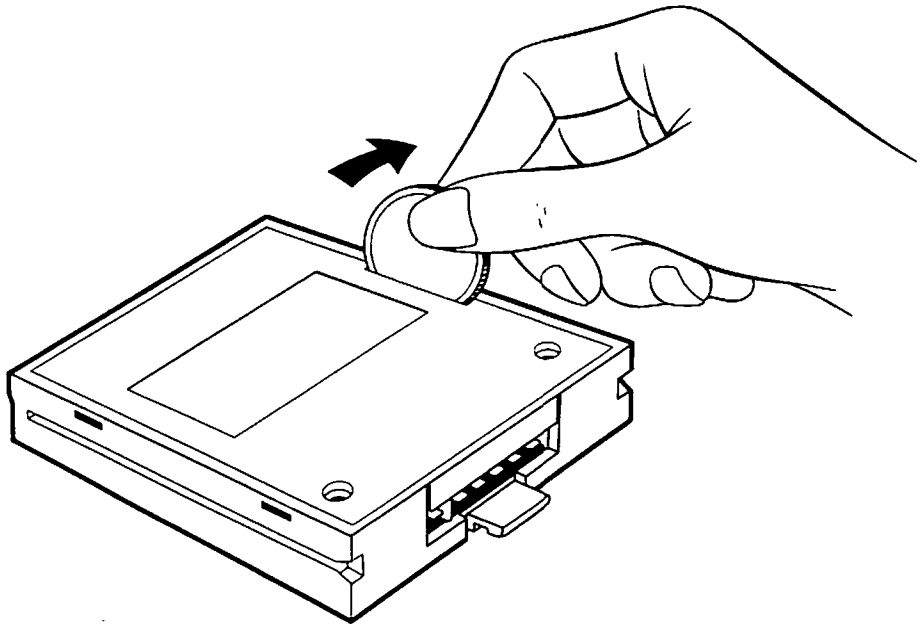
(2) Applying pressure on points A and B, slide the battery cassette out from the main unit.



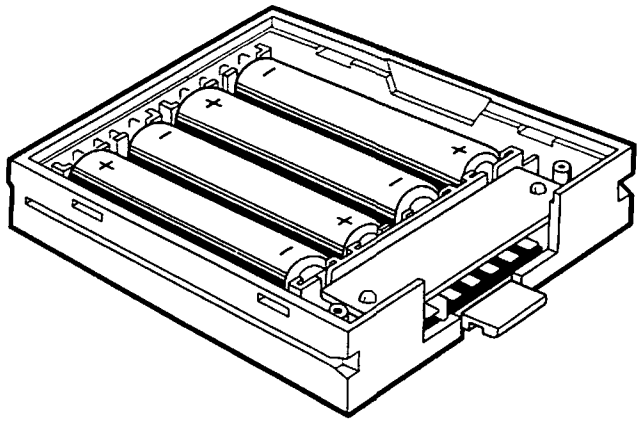
(3) Remove the battery cassette. Set it like following.



(4) Insert a coin in the guide groove, and twist to the arrow to remove the upper cover.



(5) Insert batteries. The spring side is the negative pole. Set the cells carefully like following.



(6) Replace the cover. If it closed. it snaps. Then reassemble in reverse order.

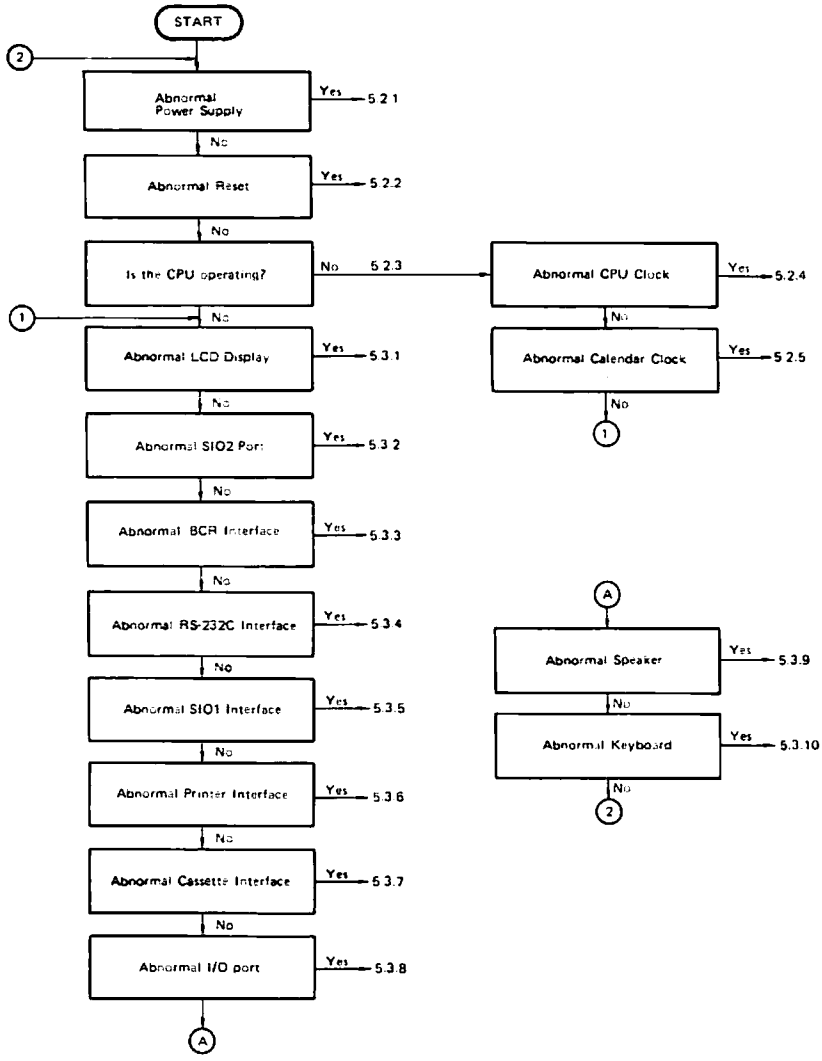
CHAPTER 5
OPERATION TEST

Preparation

The following is needed for the operations test.

(1) Oscilloscope (100 MHz)
(2) Tester
(3) Test Connector

5.1 Operations Test Flow Chart



5.2 CPU Peripheral Circuit

5.2.1 PC-8201 Power Supply Operation Test

〈Reference〉 Chapter 4 DISASSEMBLY/REASSEMBLY

(1) Measured power supply

PIN No. 3	−5 V
PIN No. 6	5 V
(within +10% to −5%)	

* If power supply operation is abnormal, see Item 6.2.1 "PC-8201 Abnormal Power Supply".

5.2.2 Reset Operation Test

As soon as the power supply is turned on or reset is depressed, the RESET signal in U17, 80C85, (P36) changes from "H" level to "L" level and the RESET OUT signal in U17 (P3) changes from "L" level to "H" level.

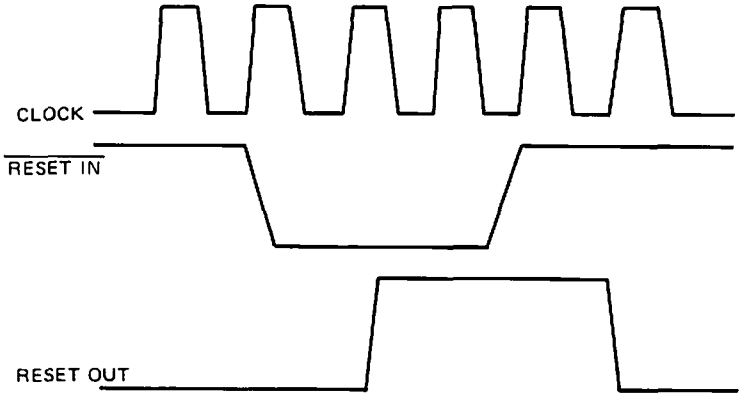


Figure 5.1 Reset Operating Test

* If reset is abnormal, see Item 6.2.2 "PC-8201 Abnormal Reset".

5.2.3 CPU (80C85) Operation Test

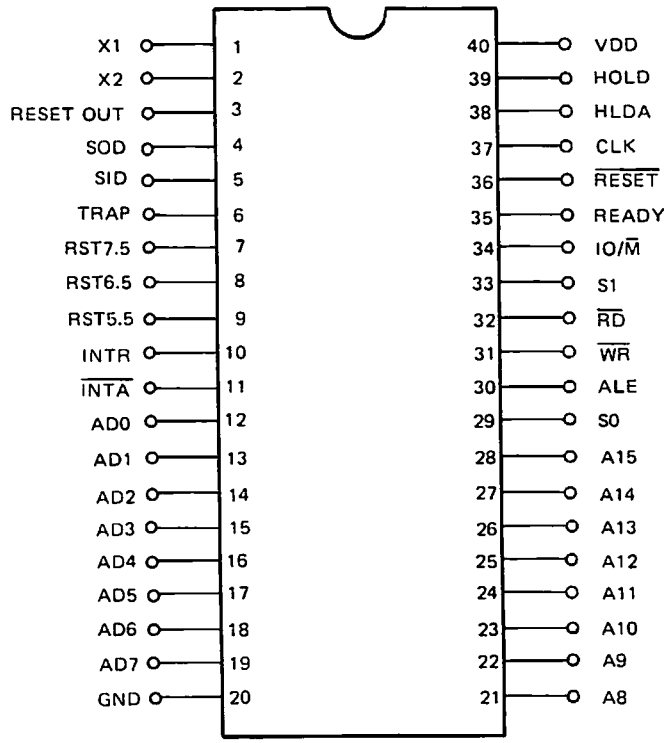


Figure 5.2 80C85 Terminal Connection (Top view)

(1) 80C85 Terminal Signals

When turning on the PC-8201 power supply or depressing the reset switch, if each terminal of U17 (80C85) operates correctly, you can confirm the pulse changing to the opposite level at each terminal.

Following signals are like next.

RESET	(P36)	"H" level	(+5 V)
RESET OUT	(P3)	"L" level	(+0 V)
HLDA	(P38)	"L" level	(+0 V)
TRAP	(P6)	"L" level	(+0 V)
VDD (+5 V)	(P40)	"H" level	(+5 V)
GND	(P20)	"L" level	(+0 V)

Then the contents of Figure 5.3 are displayed on the monitor.

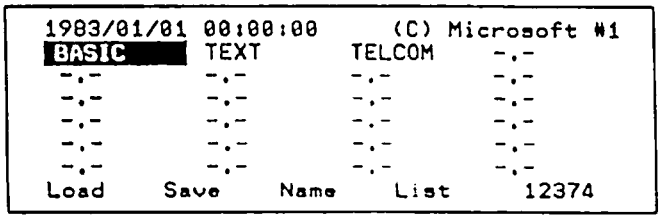


Figure 5.3 Start Message

(2) 80C85 Operation Signal

If the PC-8201 operates correctly, you can confirm the signal in Figure 5.4.

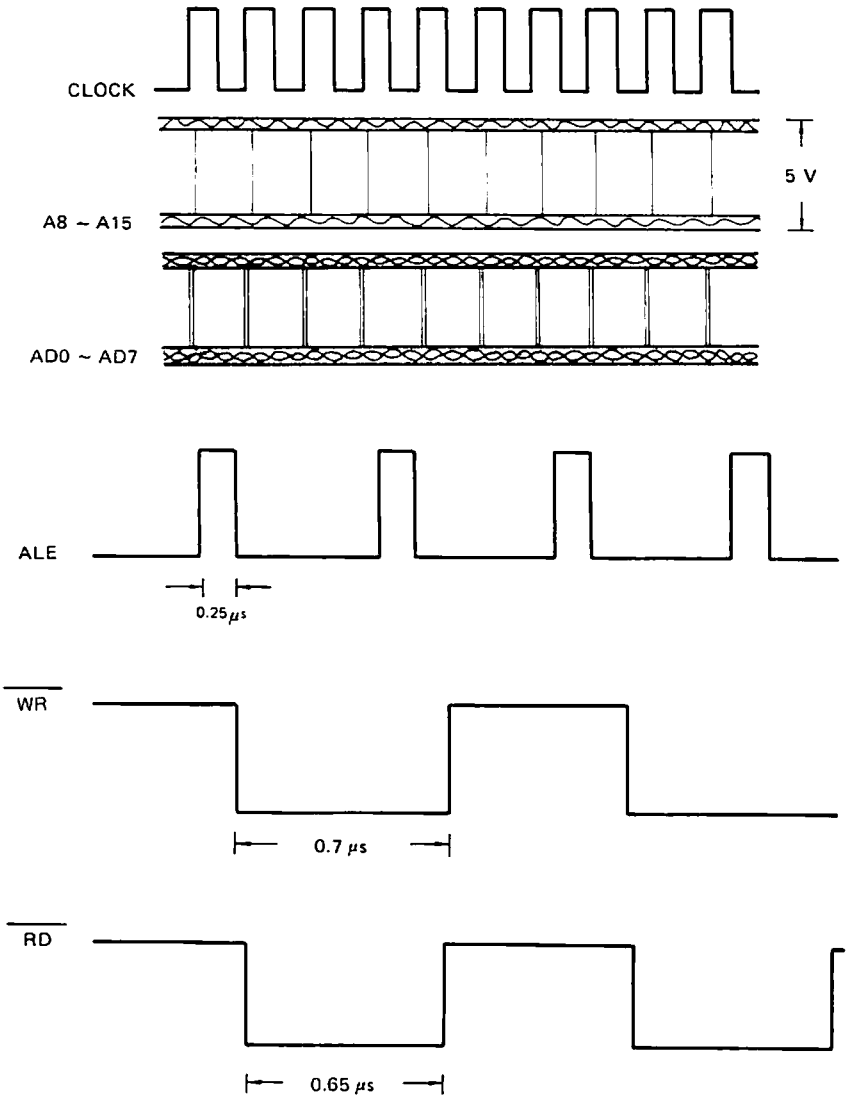


Figure 5.4 80C85 Operating Test

(If the CPU (80C85) is abnormal, see Item 6.2.3 "Abnormal CPU".)

5.2.4 CPU Clock Operation Test

Measure U17, 80C85, (P37) of the CPU clock. Figure 5.5 shows the signal at U17 (P37).

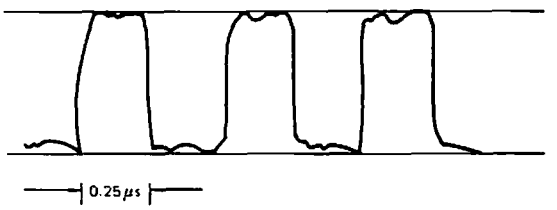


Figure 5.5 U17 (P37) Output Signal

* If CPU CLOCK is abnormal, see Item 6.2.4.

5.2.5 Calendar Clock Operation Test

Measure whether the signal in Figure 5.6 is being transmitted to U20 (P10) of calendar clock.

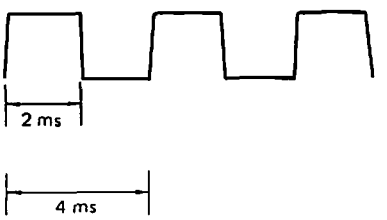


Figure 5.6 Calendar Clock Signal

〈Reference〉 Figure 5.7 "Calendar Clock Peripheral Circuit"

* If the calendar clock is abnormal, see Item 6.2.5 "Abnormal Calendar Clock".

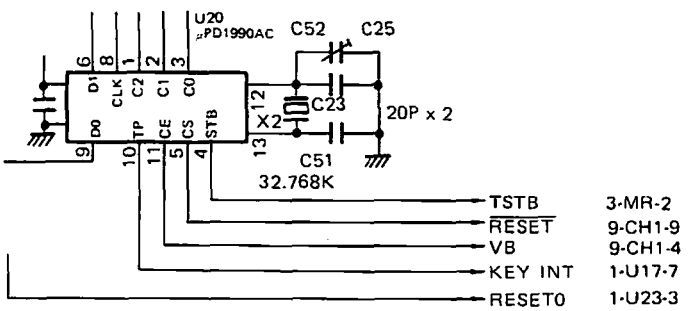


Figure 5.7 Calendar Clock Peripheral Circuit

5.3 I/O Peripheral Circuit

5.3.1 LCD Operation Test

(1) When executing the test program in Figure 5.8. LCD block in Figure 5.9 is erased and displayed in order.

```
5  PRINT CHR$(27);CHR$(85)
10 OUT 185,255:OUT 186,3
20 OUT 240,56:OUT 240,57
30 FOR N=1 TO 319:PRINT "X";:NEXT
40 FOR N=0 TO 7
50 OUT 240,56:OUT 185,255:OUT 186,3:OUT 240,57
60 OUT 240,56:OUT 185,255-2^N:OUT 240,57
70 FOR I=1 TO 600:NEXT
80 OUT 185,0  :OUT 186,0:OUT 240,57
90 NEXT:OUT 240,56
100 FOR N=0 TO 1
110 OUT 240,56:OUT 186,3-2^N:OUT 240,57
120 FOR I=1 TO 600:NEXT
125 OUT 185,255:OUT 186,3
130 NEXT
140 OUT 185,255:OUT 186,3
150 OUT 240,56:OUT 240,57
```

Figure 5.8 Test Program

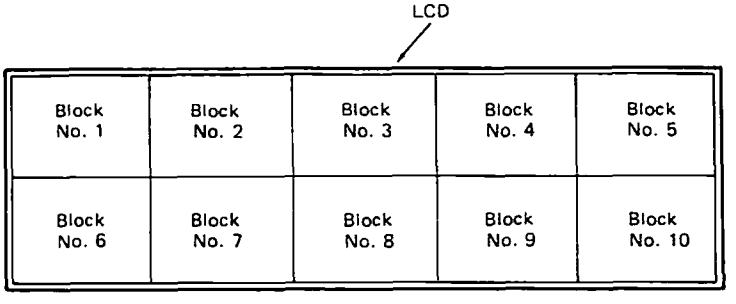


Figure 5.9 LCD Canvas

(2) By executing the test program in Figure 5.10, you can confirm the signal in Figure 5.11 on LCD connector (CN7)

```
10 PRINT "1"; : GOTO 10
```

Figure 5.10 Test Program

Figure 5.11 LCD Connector Signal

〈Reference〉 Figure 5.12 "LCD Peripheral Circuit"

* If the LCD is abnormal, see Item 6.3.1 "Abnormal LCD".

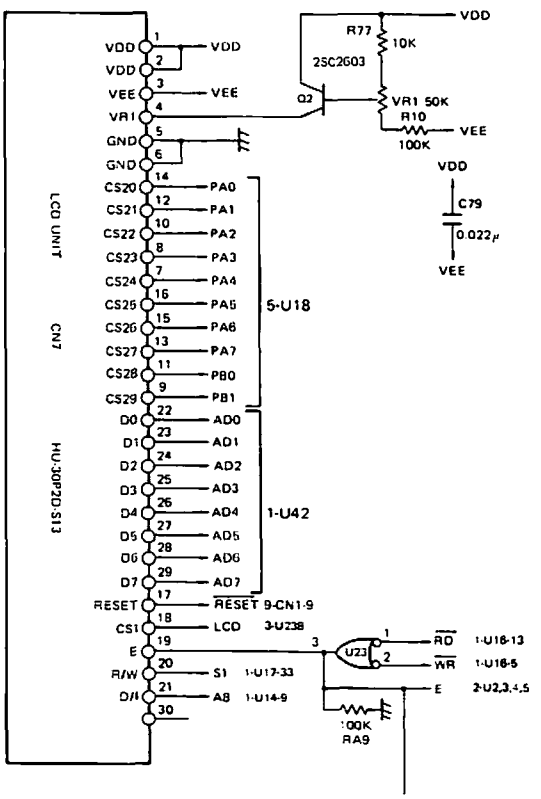


Figure 5.12 LCD Peripheral Circuit

5.3.2 SIO2 Port Operation Test

Preparation

Connect the pin in Figure 5.14 with SIO2 connector.

(1) SIO2 Port Test Program

Test using the program in Figure 5.13.

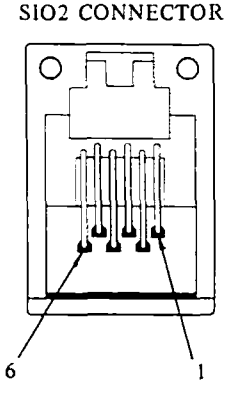
Repeat to transmit/receive the data (Addresses &H1 to &HFF), and display the received data on the monitor, then compare it with the transmitted data. If it is normal, "SIO2 TEST OK" is displayed. or "SIO2 ERROR" is displayed.

You can confirm the signal in Figure 5.15 in P2 and P3 of the SIO2 connector.

```
10 OUT 144,64:OUT 216,27
20 OUT 188,3 :OUT 189,64 :PRINT CHR$(12)
30 FOR A=1 TO 255 :OUT 200,A:B=INP(200)
31 'V=INP(216) AND 4 :IF A=4 THEN LPRINT "OKK";
40 IF A<>B GOTO 80 ELSE PRINT B;
60 NEXT
70 PRINT:PRINT "SIO2 TEST OK":END
80 PRINT:PRINT "SIO2 ERROR!!":END
```

Figure 5.13 Test Program

· SIO2 6-pin DuPont BERG modular jack



Pin number	Signal name
1	GND
2	TxD
3	RxR
4	RTS
5	CTS
6	Vcc

Figure 5.14 Connected Circuit

〈Reference〉 Figure 5.16 "Serial Interface Peripheral Circuit".

* If SIO2 is abnormal, see Item 6.3.2 "Abnormal SIO2".

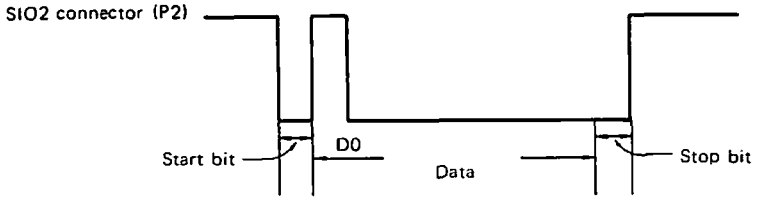


Figure 5.15 SIO2 Data Signal

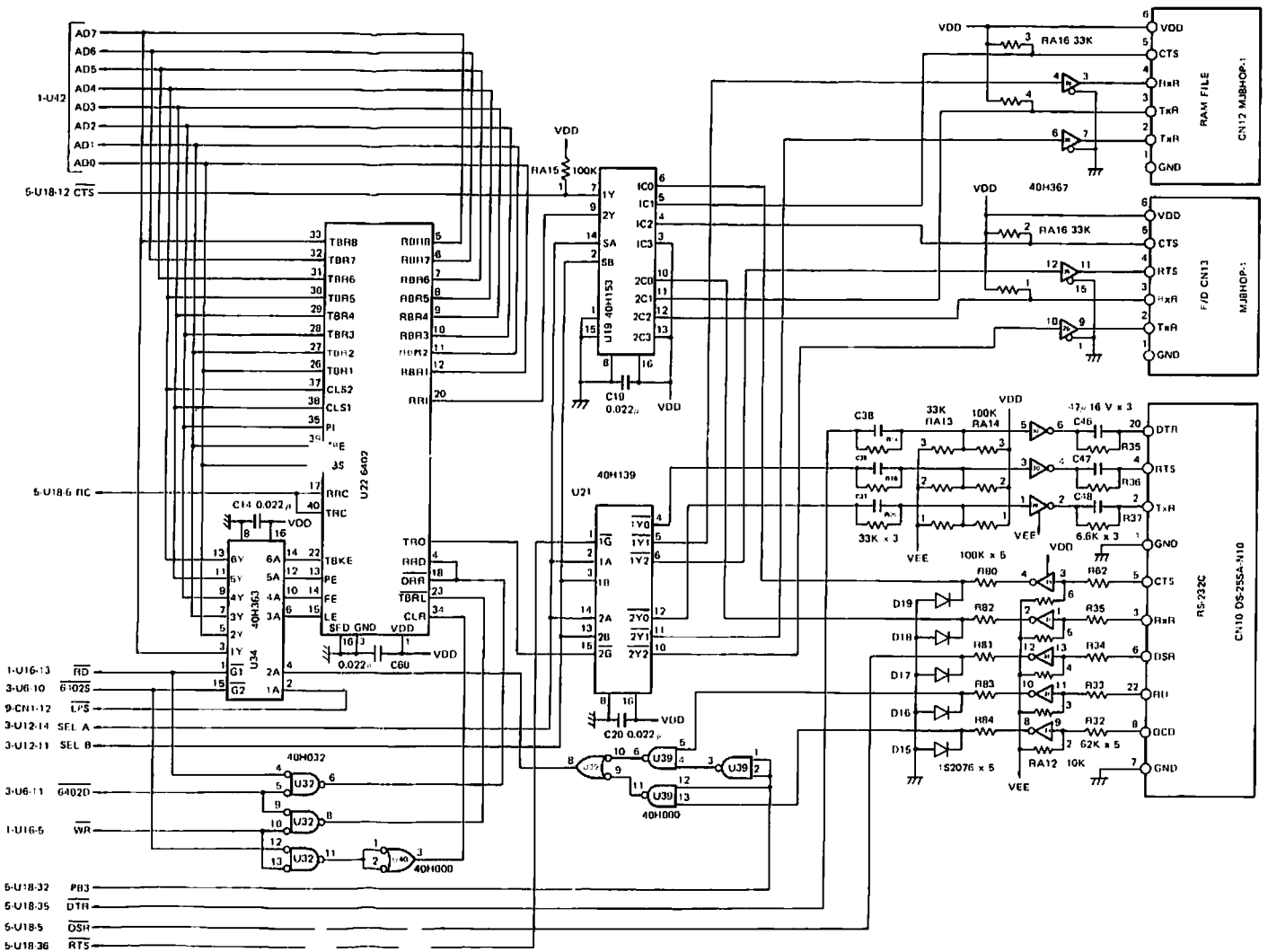


Figure 5.16 Serial Interface Peripheral Circuit

5.3.3 BCR Interface Operation Test

〈Preparation〉

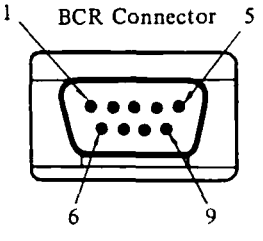
Connect the pin Figure 5.18 with the BCR connector.

(1) BCR Interface Test Program

Test using the program in Figure 5.17. If the BCR interface is normal, "BCR TEST OK" is displayed, or "BCR ERROR" is displayed. The signal in U27 (P6) changes from an "L" level to "H" level by connecting the circuit.

```
10 FOR N=1 TO 255
20 A=INP(187) AND 8
30 IF A AND 8 THEN PRINT N; ELSE GOTO 100
40 NEXT
50 PRINT :PRINT "BCR TEST OK" :END
100 PRINT :PRINT "BCR ERROR !!"
```

Figure 5.17 Test Program



Pin number	Signal name
2	R x DB
5	GND
7	GND
9	V_{cc}

Figure 5.18 Pin Connection

〈Reference〉 Figure 5.19 "BCR Peripheral circuit"

* If BCR is abnormal, see Item 6.3.3 "Abnormal BCR Interface".

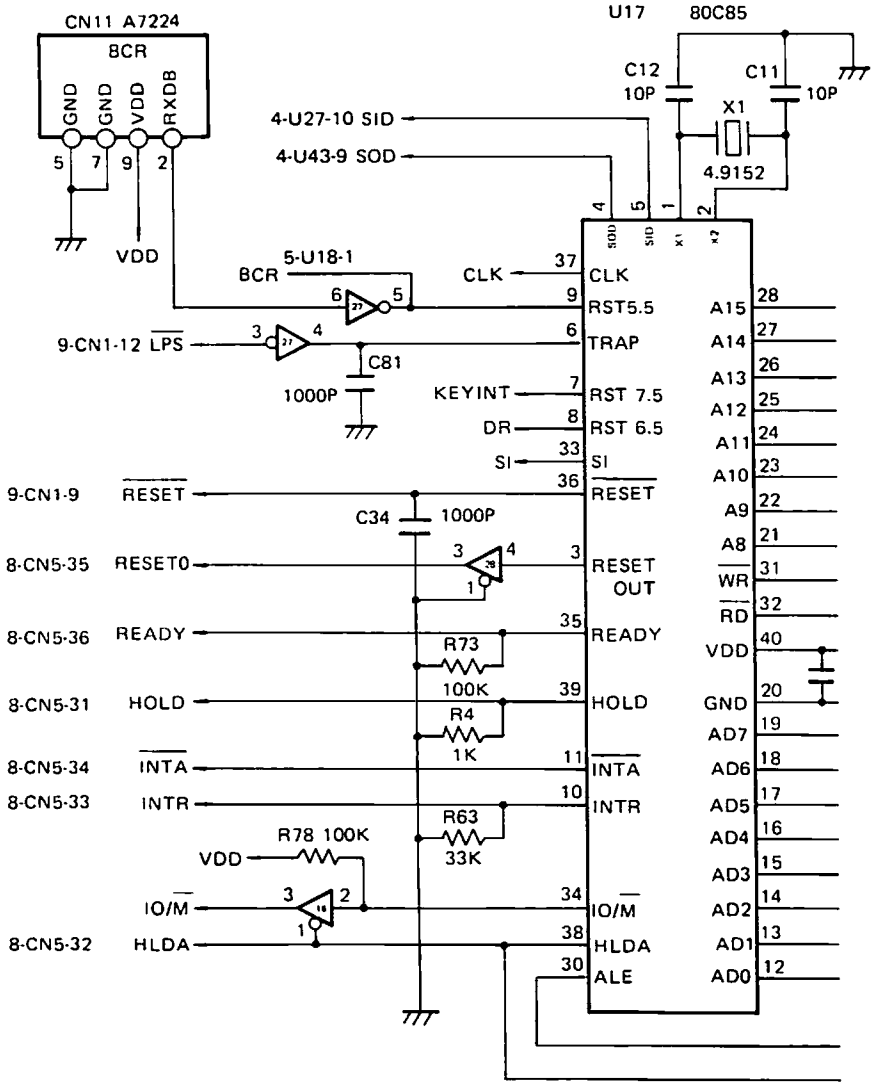


Figure 5.19 BCR Peripheral Circuit

5.3.4 RS-232C Interface Operation Test

〈Preparation〉

Connect the pin in Figure 5.21 with the RS-232C connector.

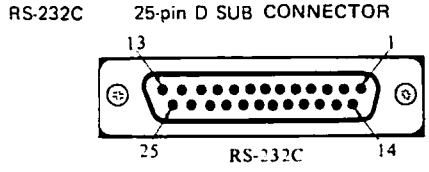
(1) RS-232C Connector Test Program

Test using the program in Figure 5.20.

Repeat transmitting and receiving the data (address &H1 to &HFF). and display the received data on the monitor. then compare it with the transmitted data. If the RS-232C interface is normal. you can confirm each terminal signal in Figure 5.22, "RS-232C TEST OK" is displayed when the test is finished. If it is abnormal, "RS-232C ERROR" is displayed.

```
10 OUT 144,192:OUT 216,27
20 OUT 188,3: OUT 189,64 :PRINT CHR$(12)
30 FOR A=1 TO 255:OUT 200,A:B=INP(200)
40 IF A<>B GOTO 80 ELSE PRINT B;
50 FOR N=1 TO 100:NEXT
60 NEXT
70 PRINT:PRINT "RS-232C TEST OK":END
80 PRINT:PRINT "RS-232C ERROR !!":END
```

Figure 5.20 Test Program



Pin number	Signal name
1	GND
2	TxD
3	RxD
4	RTS
5	CTS
6	DSR
7	GND
8	DCD
to	
20	DTR
22	RD
25	...

Figure 5.21 Pin Connection

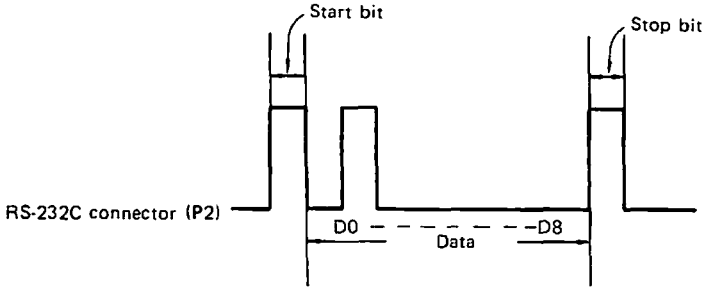


Figure 5.22 RS-232C Data Signal

〈Reference〉 Figure 5.16 Serial Interface Peripheral Circuit

* If the RS-232C is abnormal, see Item 6.3.4 "Abnormal RS-232C".

5.3.5 SIO1 Interface Operation Test

〈Preparation〉

Connect the pin in Figure 5.24 with SIO1 connector.

(1) SIO1 Interface Test Program

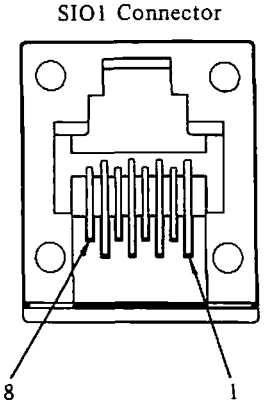
Test using the program in Figure 5.23.

Repeat transmitting and receiving the data (address &H1 to &HFF). Display the received data on the monitor, then compare it with transmitted data. If it is normal, "SIO1 TEST OK" is displayed, otherwise "SIO1 ERROR" is displayed. If SIO1 operates correctly, you can verify the signal in Figure 5.25 at the connector pin.

```
10 OUT 144,28:OUT 216,27
20 OUT 188,8 :OUT 189,64:PRINT CHR$(12)
30 FOR A=1 TO 255 :OUT 200,A:B=INP(200)
40 IF A<>B GOTO 80 ELSE PRINT B;
60 NEXT
70 PRINT:PRINT "SIO 1 TEST OK":END
80 PRINT:PRINT "SIO 1 ERROR!!":END
```

Figure 5.23 Test Program

· SIO1 8-pin DuPont BERG modular jack



Pin number	Signal name
1	GND
2	TxD
3	RxR
4	RTS
5	CTS
6	Vcc
7	NC
8	NC

Figure 5.24 Pin Connection

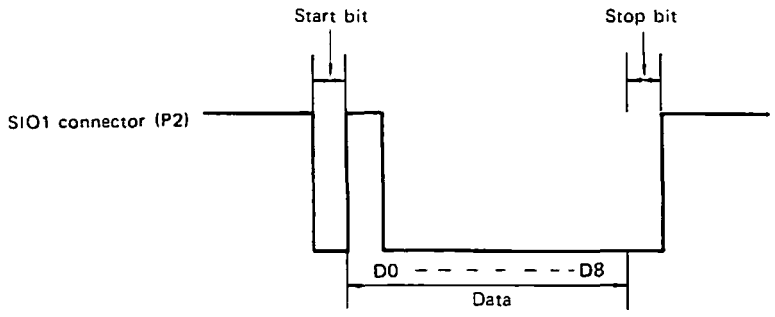


Figure 5.25 SIO1 Data Signal

(Reference) Figure 5.16 "Serial Interface Peripheral Circuit"

* If the SIO1 interface is abnormal, see Item 6.3.5 "Abnormal SIO1."

5.3.6 Printer Interface Operation Test

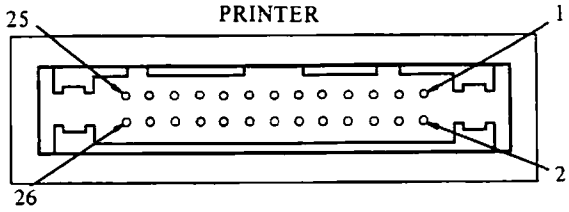
〈Preparation〉

Connect the pin in Figure 5.26 with the printer bus connector.

(1) The terminal number 1 (PSTB) transmits "H" level and the terminal number 21 (BUSY) transmits "L" level.

(2) By executing the test program in Figure 5.27, you can verify the signal in Figure 5.28.

· Printer 26-pin connector



Pin number	Signal name	Pin number	Signal name
1	STROBE	2	GND
3	PD0	4	GND
5	PD1	6	GND
7	PD2	8	GND
9	PD3	10	GND
11	PD4	12	GND
13	PD5	14	GND
15	PD6	16	GND
17	PD7	18	GND
19	NC	20	GND
21	BUSY	22	GND
23	NC	24	GND
25	SLCT	26	NC

Figure 5.26 Connected Circuit

```
10 LPRINT CHR$(255);:GOTO 10
```

Figure 5.27 Test Program

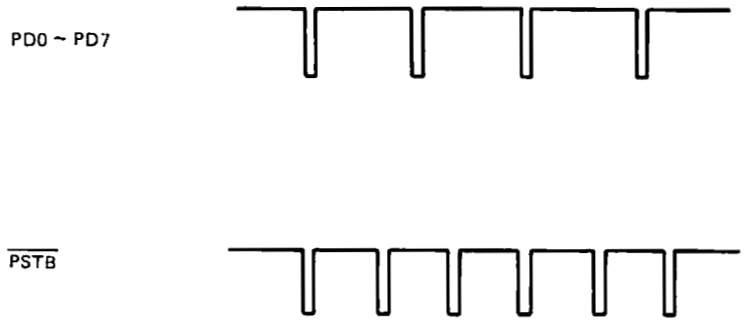


Figure 5.28 Each Terminal Signal

(Reference) Figure 5.29 "Printer Interface Peripheral Circuit"

* If the printer interface is abnormal, see Item 6.3.6 "Abnormal Printer Interface".

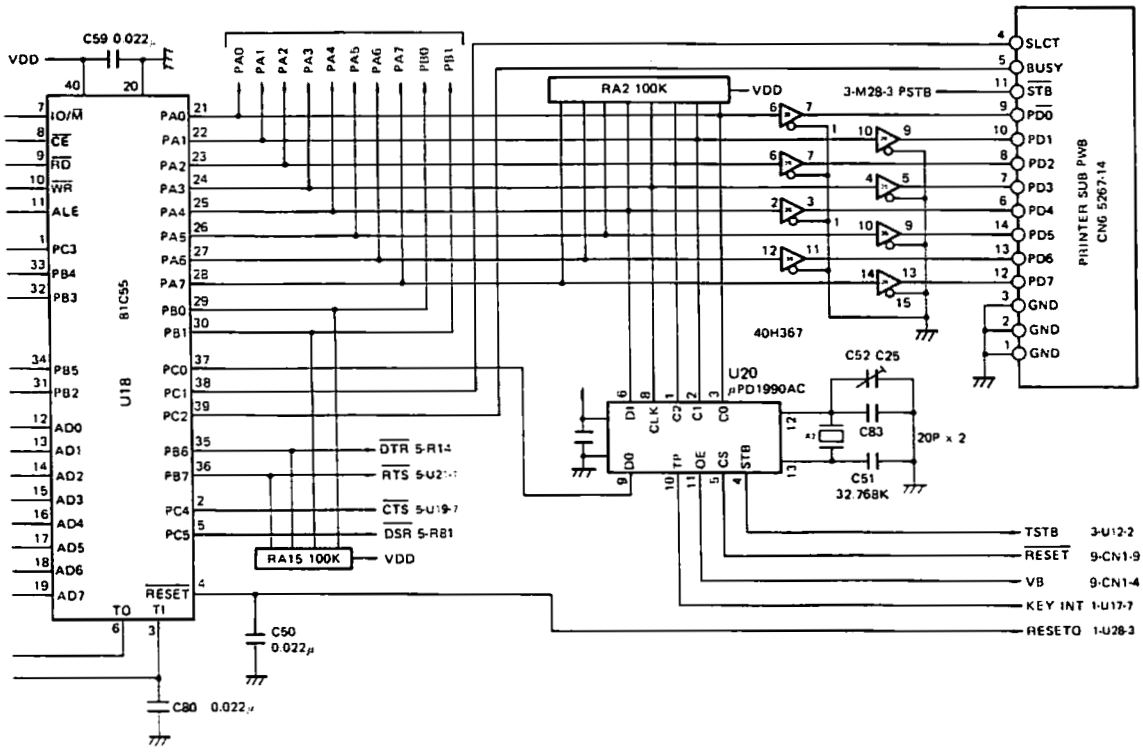


Figure 5.29 Printer Interface Peripheral Circuit

5.3.7 Audio Cassette Interface Operation Test

(1) REC Operating Test
By executing the test command in Figure 5.30, you can verify the signal in Figure 5.31.

```
CSAVE "X"
```

Figure 5.30 Test Command

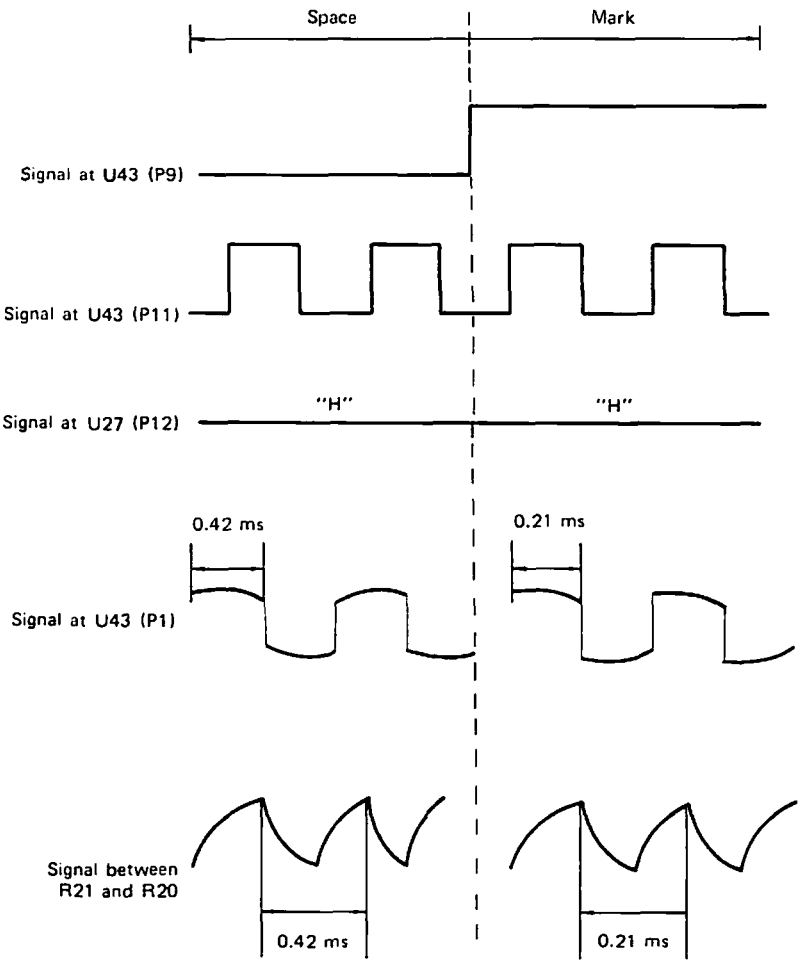
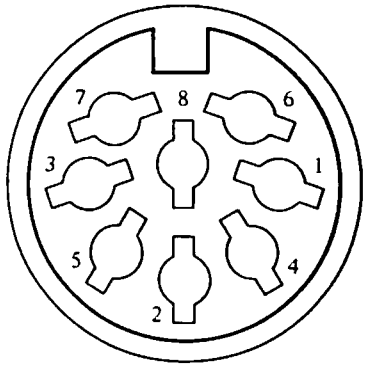


Figure 5.31 Terminal Signals

(2) MON Operation Test

〈Preparation〉
Connect the pin in Figure 5.32 with the cassette connector.

a) By connecting the circuit, you can measure the signal in Figure 5.33.



Pin number	Signal name
1	T x C
2	GND
3	GND
4	MIC
5	EAR
6	REM1
7	REM2
8	Vcc

Figure 5.32 Pin Connection

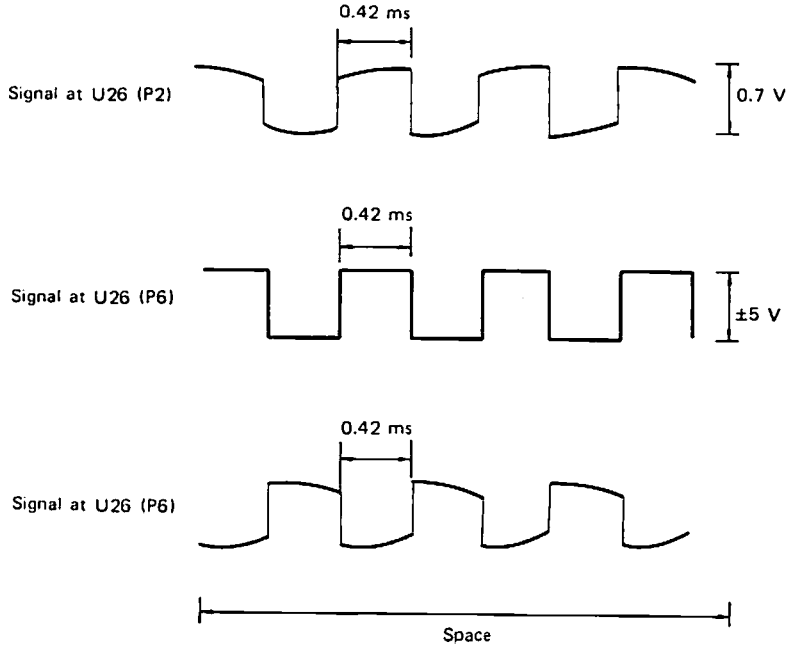


Figure 5.33 Terminal Signals

b) By executing the test command in Figure 5.34, you can measure the signal in Figure 5.35.

```
CSAVE "X"
```

Figure 5.34 Test Command

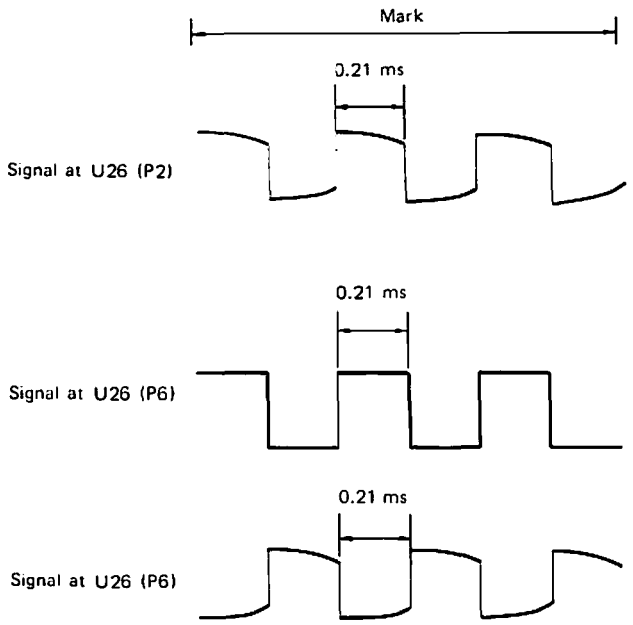


Figure 5.35 Terminal Signals

〈Reference〉 Figure 5.36 "Audio Cassette Interface Peripheral Circuit"

* If the Audio cassette interface is abnormal, see Item 6.3.7 "Abnormal Audio Cassette Interface".

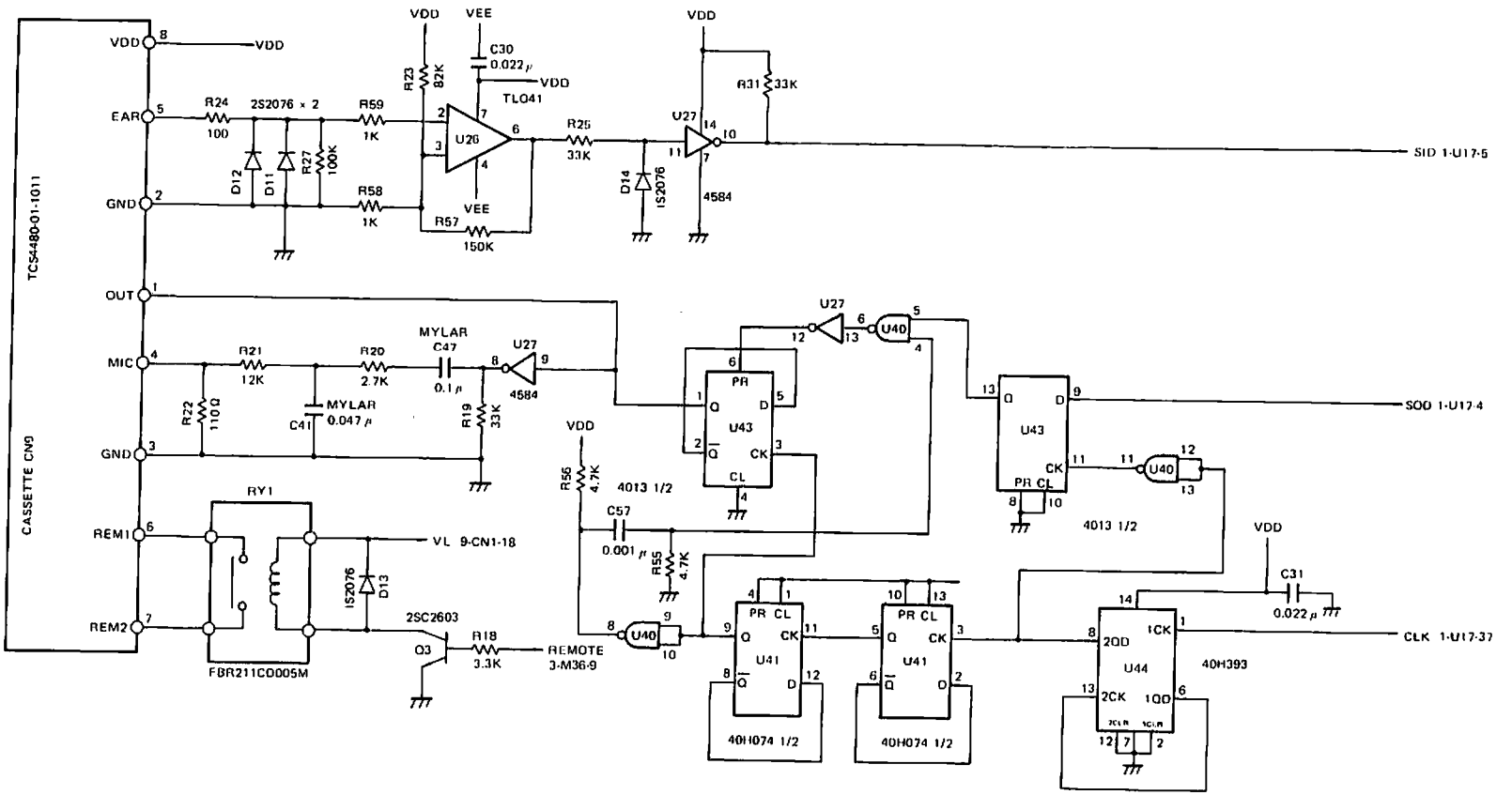


Figure 5.36 Audio Cassette Interface Peripheral Circuit

5.3.8 I/O Port Operation Test

* If the operating test is abnormal, see Item 6.3.8 "Abnormal I/O Port".

〈Reference〉 Figure ROM peripheral circuit
Figure 81C55 peripheral circuit
Figure 6402 peripheral circuit

(1) OUT 90H Operating Test
By executing the test program in Figure 5.37, the signal at U36 (P9) changes from "L" level to "H" level.

```
10 OUT 144,8
```

Figure 5.37 Test Program

(2) OUT A1H Operating Test
If pushing the SHIFT-key and the BANK-key at the same time in MENU mode, you can confirm the signal shown in Figure 5.38 in U53 (P1).

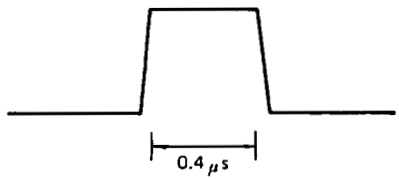


Figure 5.38 Signal in U53 (P1)

(3) IN A0H Operation Test
By pushing the SHIFT-key and the BANK-key at the same time in MENU mode, the signal in U11 (P2) changes from "L" level to the signal shown in Figure 5.39.

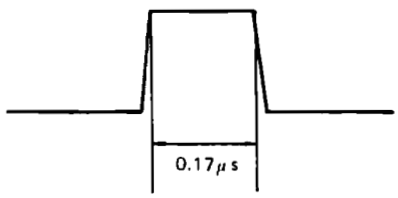


Figure 5.39 Signal in U11 (P1)

(4) OUT B9H Operation Test
By executing the test program in Figure 5.40, you can confirm the signal shown in Figure 5.41 in U18 (P21).

```
10 GOTO 10
```

Figure 5.40 Test Program

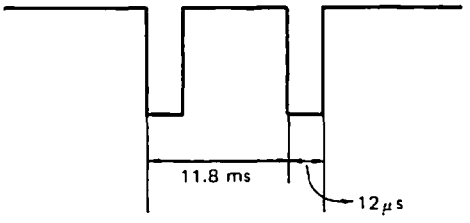


Figure 5.41 Signal in U18 (P21)

(5) OUT BAH Operation Test
By executing the test program in Figure 5.42, the signal in U18 (P31) changes from "H" level to "L" level.

```
10 OUT 186,0
```

Figure 5.42 Test Program

(6) IN BBH Operation Test
You can confirm the signal shown in Figure 5.43 in U18 (P37).

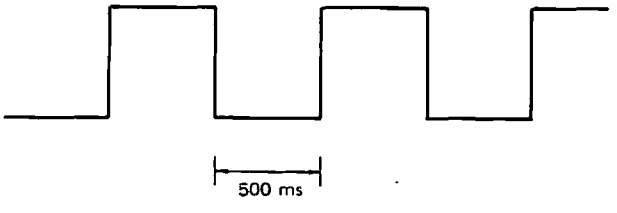


Figure 5.43 Signal in U18 (P37)

(7) IN/OUT C8H Operation Test

〈Preparation〉
Connect the pin 2 of the RS-232C connector with the pin 3. (See Figure 5.21 "Pin connection" of item "RS-232C Interface Operating Test".
By executing the test program in Figure 5.44, you can confirm the signal shown in Figure 5.45 in U21 (P12).

```
10 OUT 144,192:OUT 216,3
20 OUT 183,3 :OUT 189,64:PRINT CHR$(12)
30 A=9 :OUT 200,A:B=INP(200)
40 IF A<>B GOTO 80 ELSE PRINT B;
70 GOTO 30
80 PRINT "ERROR"
```

Figure 5.44 Test Program

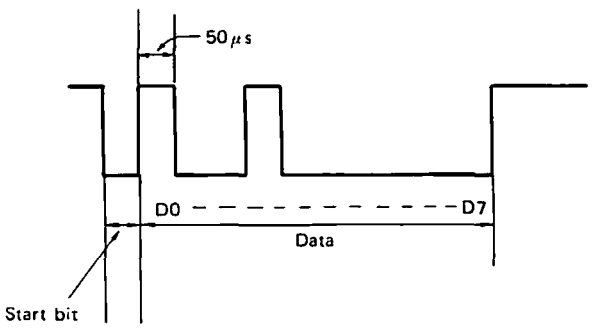


Figure 5.45 Signal in U21 (P12)

(8) OUT D8 Operation Test

〈Preparation〉
Connect the pin 2 of the RS-232C connector with the pin 3. (See Figure 5.21 "Pin Connection" of item "RS-232C Interface Operating Test".
By executing the test program in Figure 5.46, you can confirm the signal shown in Figure 5.47 in U21 (P12).

```
10 OUT 144,192:OUT 216,27
20 OUT 183,3 :OUT 189,64:PRINT CHR$(12)
30 A=9 :OUT 200,A:B=INP(200)
40 IF A<>B GOTO 80 ELSE PRINT B;
70 GOTO 30
80 PRINT "ERROR"
```

Figure 5.46 Test Program

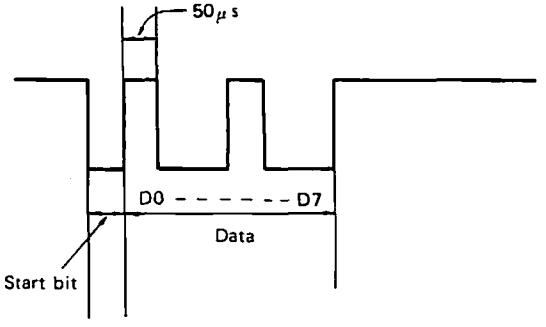


Figure 5.47 Signal in U21 (P12)

(9) IN D8H Operation Test

a) When switching the power switch from OFF to ON, the signal in U34 (P2) changes from "L" level to "H" level.

b) Execute the test program in Figure 5.48; if IN D8H is normal, "128" is displayed.

```
10 PRINT INP(216) AND 128
```

Figure 5.48 Test Program

5.3.9 Speaker Operation Test

(1) Speaker Operation Test Program
Test using the program in Figure 5.49. If the speaker is normal, it repeats ON and OFF.

```
10    BEEP
20    GOTO 10
```

Figure 5.49

5.3.10 Keyboard Operation Test

(1) Push all key-switches, and verify that the character is displayed on the LCD when pushing character key-switch and that the special functions operate correctly when pushing special function key-switches.

CHAPTER 6
TROUBLESHOOTING

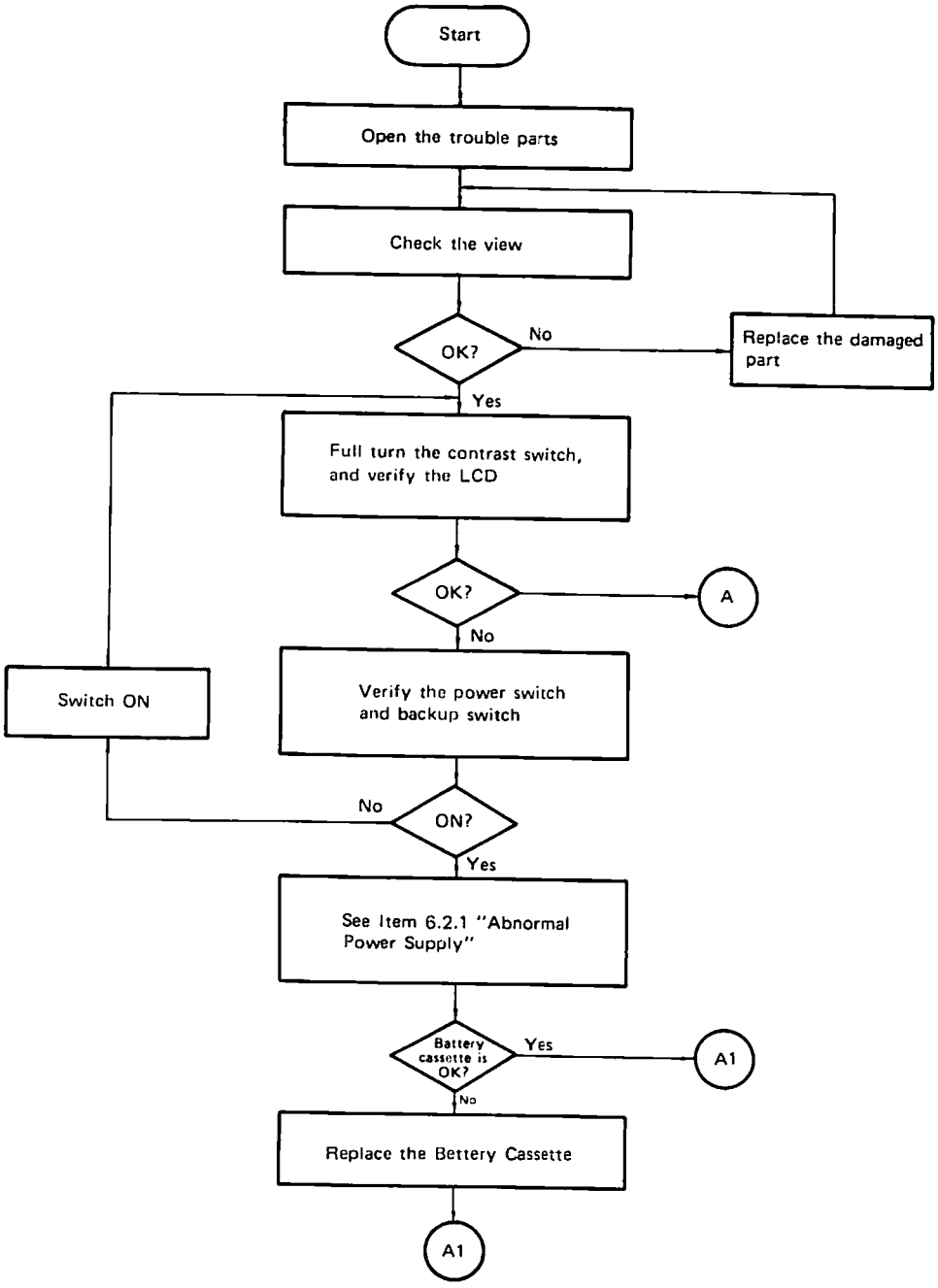
This chapter explains primary defects and how to troubleshoot them. It is impossible to explain all problems, so we hope this chapter will help you in your maintenance.

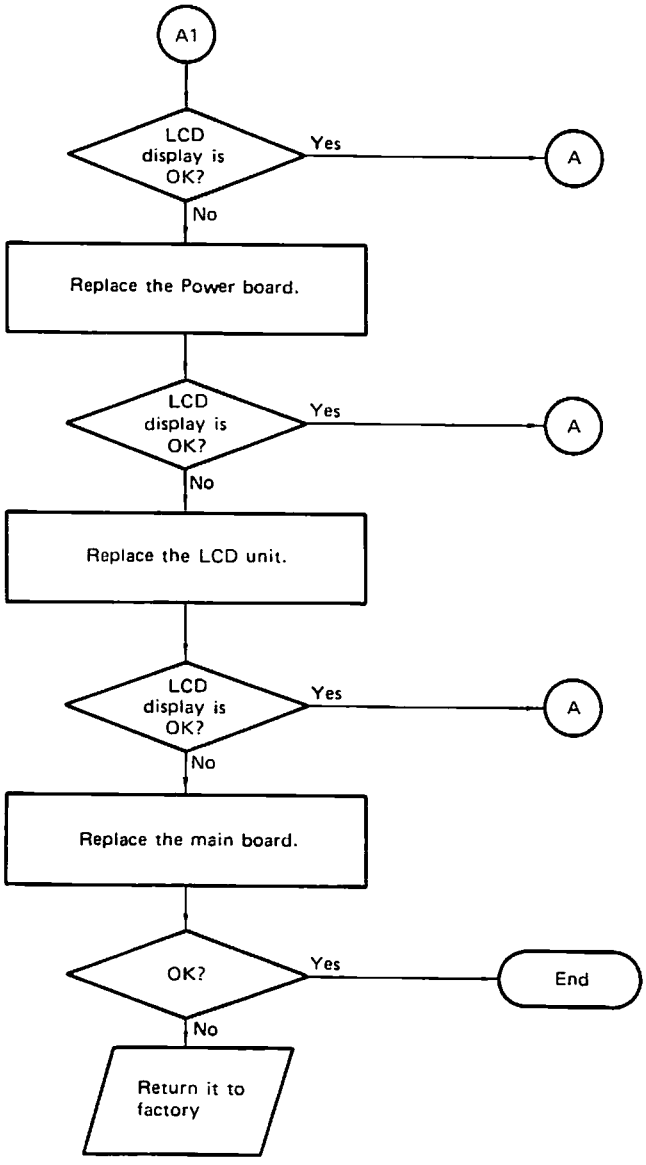
Repairing

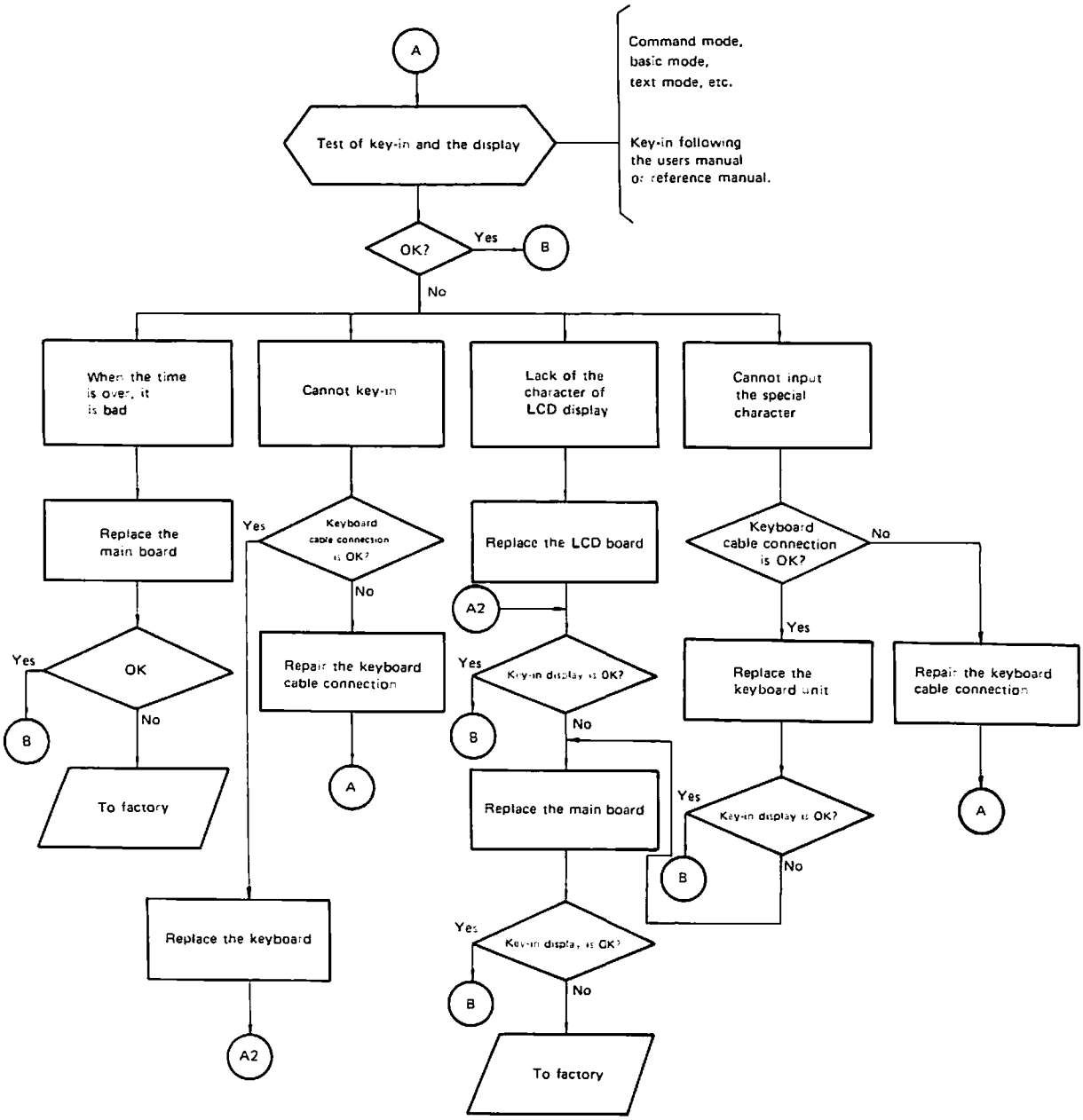
* Clear the user's claim, and describe it in a reception or a report.
* Describe the accessories in a reception.
* Repairing the instruments which have set switches such as mode, notes the switch condition.
* Check the view.
* If it is damaged, according the claim, repair it. If the damage does not accord the claim, repair it after consulting the user.

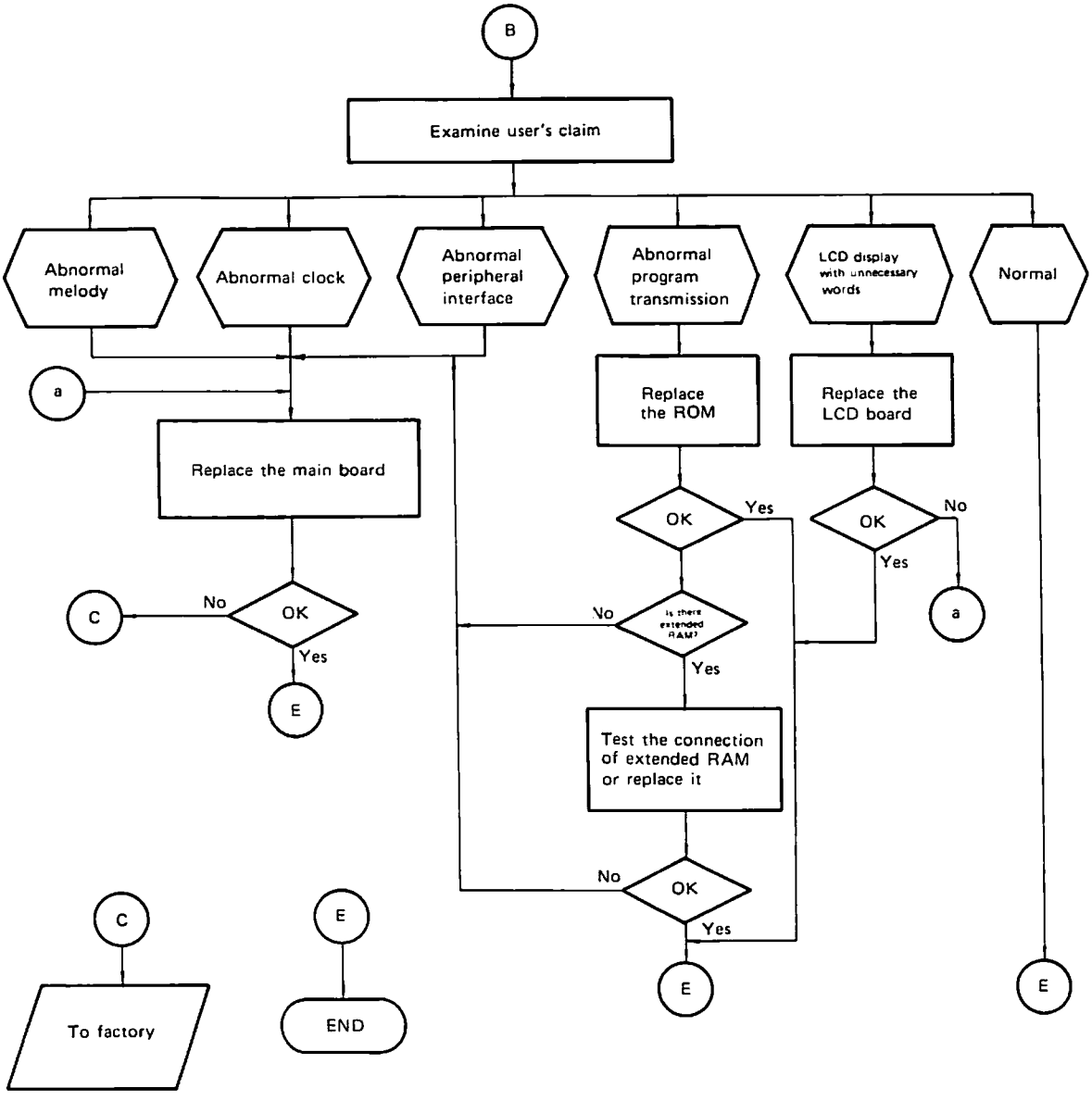
〈Reference〉 CHAPTER 4 DISASSEMBLY/REASSEMBLY
CHAPTER 5 OPERATING TEST

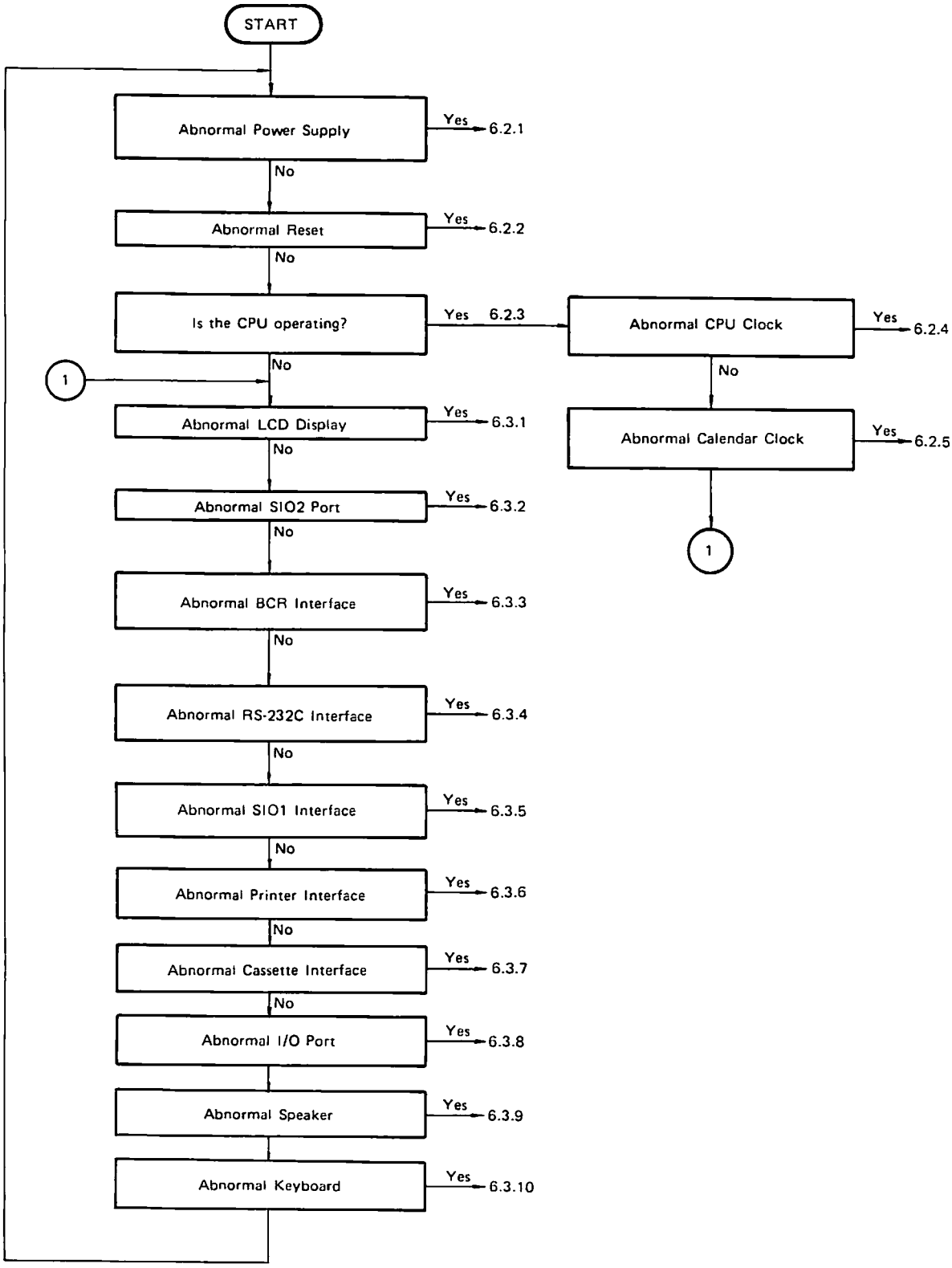
6.1 Troubleshooting Flowchart




A1
LCD display is OK?
Yes
A
No
Replace the Power board.
LCD display is OK?
Yes
A
No
Replace the LCD unit.
LCD display is OK?
Yes
A
No
Replace the main board.
OK?
Yes
End
No
Return it to factory


A
Test of key-in and the display
Command mode,
basic mode,
text mode, etc.
Key-in following
the users manual
or reference manual.
OK?
Yes
B
No
When the time is over, it is bad
Cannot key-in
Lack of the character of LCD display
Cannot input the special character
Replace the main board
Keyboard cable connection is OK?
Replace the LCD board
Keyboard cable connection is OK?
Yes
No
A2
Yes
OK
No
B
To factory
Repair the keyboard cable connection
A
Key-in display is OK?
Replace the keyboard unit
Repair the keyboard cable connection
Replace the main board
Replace the keyboard
Key-in display is OK?
To factory


B
Examine user's claim
Abnormal melody
Abnormal clock
Abnormal peripheral interface
Abnormal program transmission
LCD display with unnecessary words
Normal
a
Replace the main board
Replace the ROM
Replace the LCD board
OK
Yes
No
OK
Yes
No
C
No
OK
Yes
E
No
Is there extended RAM?
Yes
Test the connection of extended RAM or replace it
No
OK
Yes
E
a
C
To factory
E
END
E


START
Abnormal Power Supply
Yes
6.2.1
No
Abnormal Reset
Yes
6.2.2
No
Is the CPU operating?
Yes
6.2.3
Abnormal CPU Clock
Yes
6.2.4
No
1
No
Abnormal LCD Display
Yes
6.3.1
Abnormal Calendar Clock
Yes
6.2.5
No
Abnormal SIO2 Port
Yes
6.3.2
1
No
Abnormal BCR Interface
Yes
6.3.3
No
Abnormal RS-232C Interface
Yes
6.3.4
No
Abnormal SIO1 Interface
Yes
6.3.5
No
Abnormal Printer Interface
Yes
6.3.6
No
Abnormal Cassette Interface
Yes
6.3.7
No
Abnormal I/O Port
Yes
6.3.8
Abnormal Speaker
Yes
6.3.9
Abnormal Keyboard
Yes
6.3.10

6.2 CPU Peripheral Circuit

6.2.1 PC-8201 Abnormal Power Supply

Turn on PC-8201 power.

Symptoms
Nothing is displayed on the LCD.

(1) Process of checking

a) When using a battery
   1: Is the voltage of the battery cassette 6 V?
   2: Is 6 V of power being transmitted to CN3 (P3) on the power board?

b) When using a DC adapter
   1: Is the 9 V power supplied to DC adapter?
   2: Is the 9 V power supplied to CN3 (P3) on the power board?
   If it is not supplied there, the adapter jack connection is bad or D8 is bad.

c) When using a battery or DC adapter
   1: Is the signal transmitted to each part in Figure 6.1?

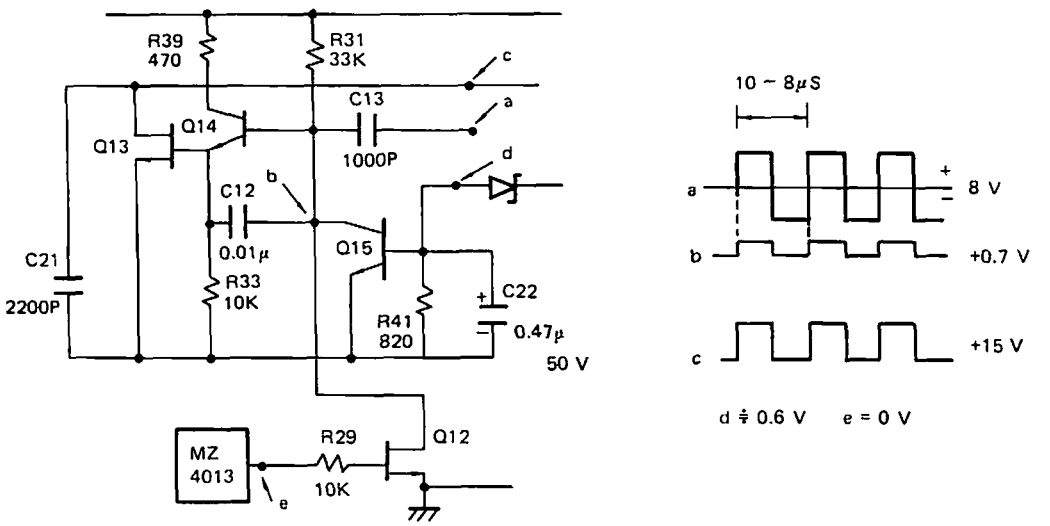


Figure 6.1 Power Supply Circuit, Output Signal

d) Is the voltage power supplied to each pin of CN1?

6	---	5 V
3	---	–5 V
4	---	5 V
5	---	GND
12	---	5 V
16	---	6 V
18	---	9 V

If the voltage is not supplied to these pins, the power board is bad.

6.2.2 PC-8201 Abnormal Reset

Symptoms

Always at reset state.
(CN1 (P9) keeps "L" level.)

a) If CN (P10) is less than 7.5 V power, U2, Q16, C1, or D7 of power board are bad.

b) If the collector of Transistor 2 is not "L" level, transistor 2 is bad.

Symptoms

Reset is not enabled at power-on.

a) When pushing a reset switch, if reset does not operate, the reset switch is bad.

b) Check the collectors of transistors 2 and 1.

6.2.3 PC-8201 Abnormal CPU (80C85)

Symptoms

The CPU does not operate.

* See Item 5.1.3 "CPU (80C85) Operation Test".

If you can verify following abnormalities, exchange the CPU board.

(1) Causes:
   a) RESET (P36) is "L" level.
   b) READY is "L" level.
   c) Clock keeps "L" level or "H" level.
      (See Item 5.1.3 "CPU Clock Operation Test".)

6.2.4 Abnormal CPU Clock

Symptoms

The CPU does not operate.

If you can verify following abnormalities, exchange the CPU board.

a) When you cannot verify the correct signal at U17 (P37).

b) If there is no signal at U17 (P1, P2), then U17, the crystal transmitter, C12, or C11 are bad.

6.2.5 Abnormal Calendar Clock

* See Item 5.1.5 "Calendar Clock Operation Test".

If you can verify following abnormalities, exchange the CPU board.

a) If you cannot verify the correct signal in U10 (P10), then U10 is bad.

6.3 I/O Peripheral Circuit

6.3.1 Abnormal LCD Display

* See Item 5.2.1 "LCD Operation Test".

If you can verify following abnormalities, exchange the LCD board.

a) If you can verify the correct signal at the LCD connector, the LCD board is bad.

b) If the correct signal is not at the LCD connector, U18, U42, U23, U16, U2, U3, U4, U5, U17, or U14 are bad.

6.3.2 Abnormal SIO2 Port

* See Item 5.2.2 "SIO2 Port Operation Test".

If you can verify following abnormalities, exchange the CPU board.

a) If something is abnormal when executing the general port operating test program (when "SIO ERROR" is displayed), U25, U21, or U22 are bad.

6.3.3 Abnormal BCR Interface

* See Item 5.2.3 "BCR Interface Operation Test".

If you can verify following abnormalities, exchange the CPU board.

a) If something is abnormal when executing the BCR operating test program (when "BCR ERROR" is displayed), U27 is bad.

6.3.4 Abnormal RS-232C Interface

* See Item 5.2.4 "RS-232C Interface Operation Test".

If you can verify following abnormalities, exchange the CPU board.

a) If something is abnormal when executing the RS-232C operating test program (when "RS-232C ERROR" is displayed), U30, U31, U21, U19, or U22 are bad.

6.3.5 Abnormal SIO1 Interface

* See Item 5.2.5 "SIO1 Interface Operation Test".

If you can verify following abnormalities, exchange the CPU board.

a) If something is abnormal when executing the SIO1 interface operating test program (when "SIO1 ERROR" is displayed), U25, U19, U21, or U22 are bad.

6.3.6 Abnormal Printer Interface

* See Item 5.2.6 "Printer Interface Operation Test".

If you can verify following abnormalities, exchange the CPU board.

a) If the data signal (PDB0 to PDB7) is abnormal, confirm the signal in U28 and in U35.

   If they are normal, the printer bus connector is bad.
   If they are abnormal, U28 or U35 are bad.

b) If PSTB signal is abnormal, confirm the signal in U12 (P2).

   If it is normal, the printer bus connector is bad.
   If it is abnormal, U12 is bad.

c) If BUSY signal is abnormal, confirm the signal in U18 (P39).

   If it is normal, the printer connector is bad.
   If it is abnormal, U18 is bad.

6.3.7 Abnormal Audio Cassette Interface

* See Item 5.2.7 "Audio Cassette Interface Operation Test".

If you cannot verify the correct signal when executing the audio cassette interface operating test program, the cause is listed below.

a) If REM+ and REM− are opened while REM is operating, RL (relay) is bad.

b) If the REC operating test, the MON operating test and the REM operating test are all normal and WRITE or READ to the audio cassette is abnormal, the cause is listed below.

* Cassette bus connector is bad.

* U43, U41, U44, or U27, of serial interface circuit are bad, and U26 is bad.

6.3.8 Abnormal I/O Port

* See Item 5.2.8 "I/O Port Operation Test".

If you can verify following abnormalities, exchange the CPU board.

a) OUT 90H is abnormal
If the output signal at U36 (P9) is abnormal, U36 or U33 are bad.

b) OUT A1H is abnormal
If the output signal at U53 (P1) is abnormal, U33, U11, or U53 are bad.

c) IN A0H is abnormal
If the output signal at U11 (P2) is abnormal, U11 or U33 are bad.

d) OUT B9H is abnormal
If the output signal at U18 (P21) is abnormal, U18 is bad.

e) OUT BAH is abnormal
If the output signal at U18 (P31) is abnormal, U18 is bad.

f) IN BBH is abnormal
If the output signal at U18 (P37) is abnormal, U20 is bad.

g) OUT C8H is abnormal
If the output signal at U21 (P12) is abnormal, U21 is bad.

h) IN C8H is abnormal
If the output signal at U19 (P10) is abnormal, U31 is bad.

i) OUT D8H is abnormal
If the output signal at U21 (P12) is abnormal, U21 is bad.

j) IN D8H is abnormal
If the output signal at U19 (P6) is abnormal, U19 is bad.

6.3.9 Abnormal Speaker

* See Item 5.2.9 "Speaker Operation Test".

(1) When the speaker doesn't operate:
Test using the operation program.

a) If the signal in figure is transmitted to U18 (P31), exchange the speaker.

b) If the signal in U18 (P31) stays low, exchange the CPU board.

(2) When the speaker doesn't stop the operation:

a) Exchange the CPU board.

6.3.10 Abnormal Keyboard

* See Item 5.2.10 "Keyboard Operation Test".

Abnormal Symptom

Though only one key is pushed, more than two characters are displayed.

(1) The cause is chattering of keyboard, so exchange the keyboard.

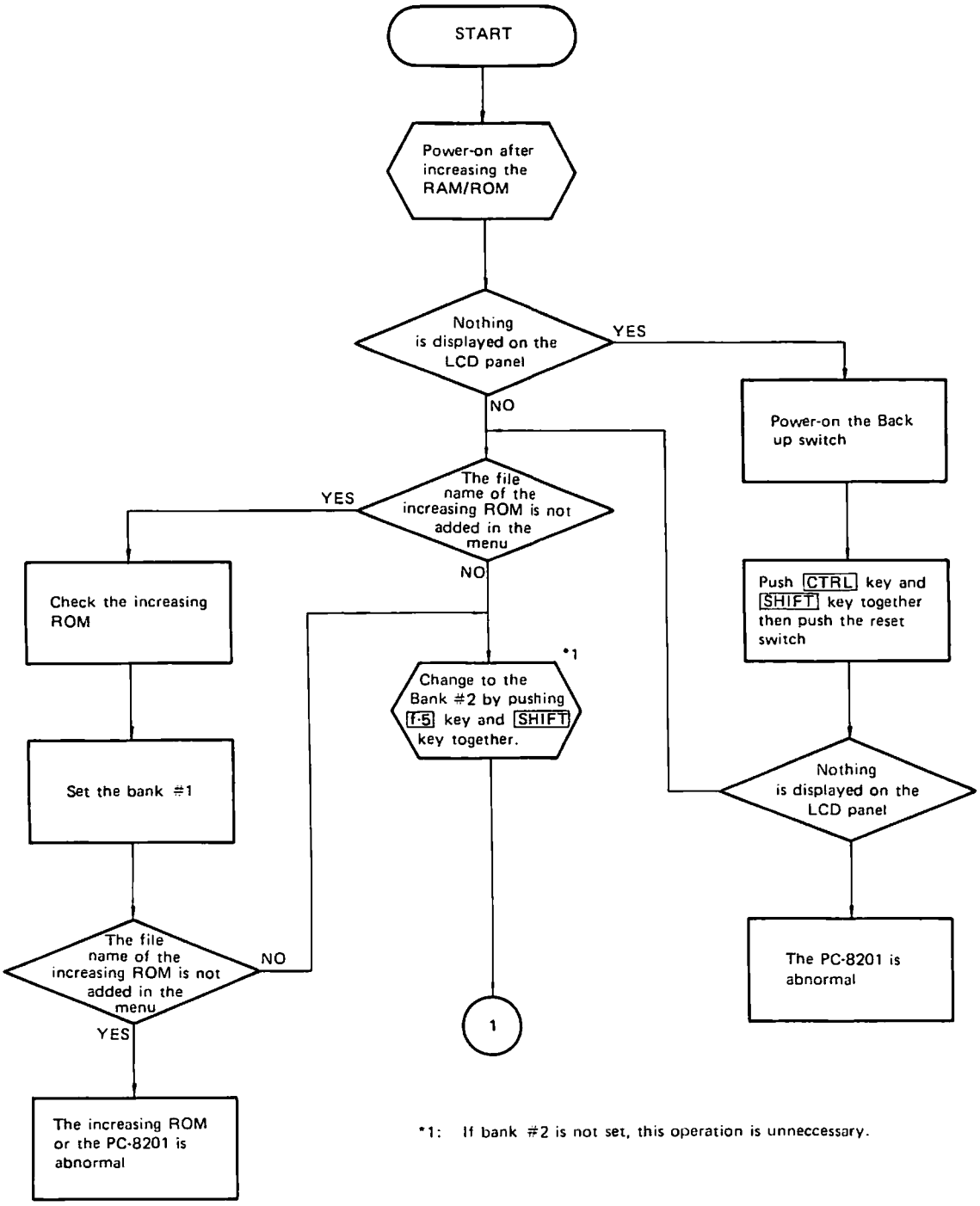
Abnormal Symptom

Nothing is displayed on the LCD.

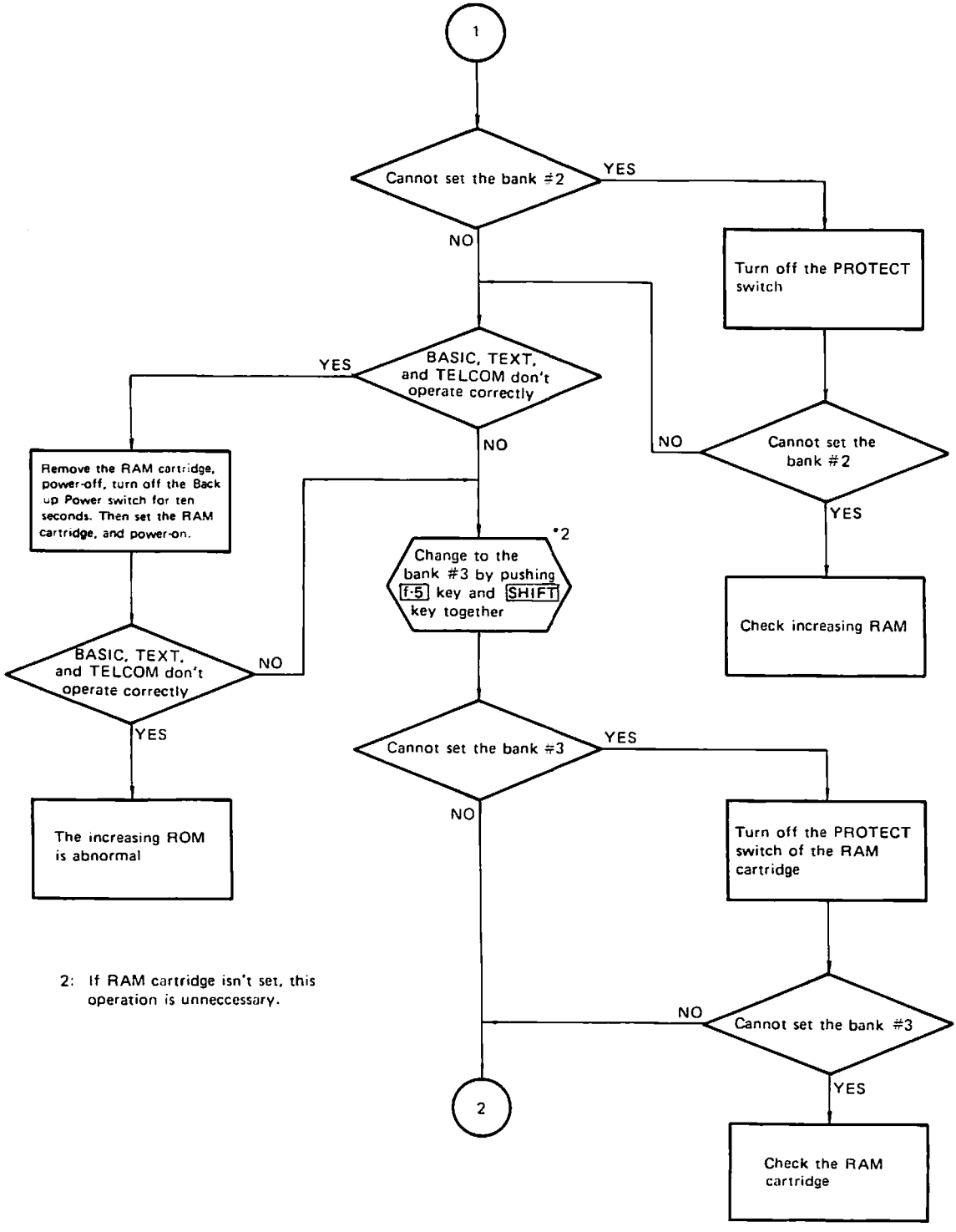
(1) If specific character is not displayed, the key-switch is bad. Exchange the key-switch.

(2) If all characters are not displayed, exchange the CPU board.

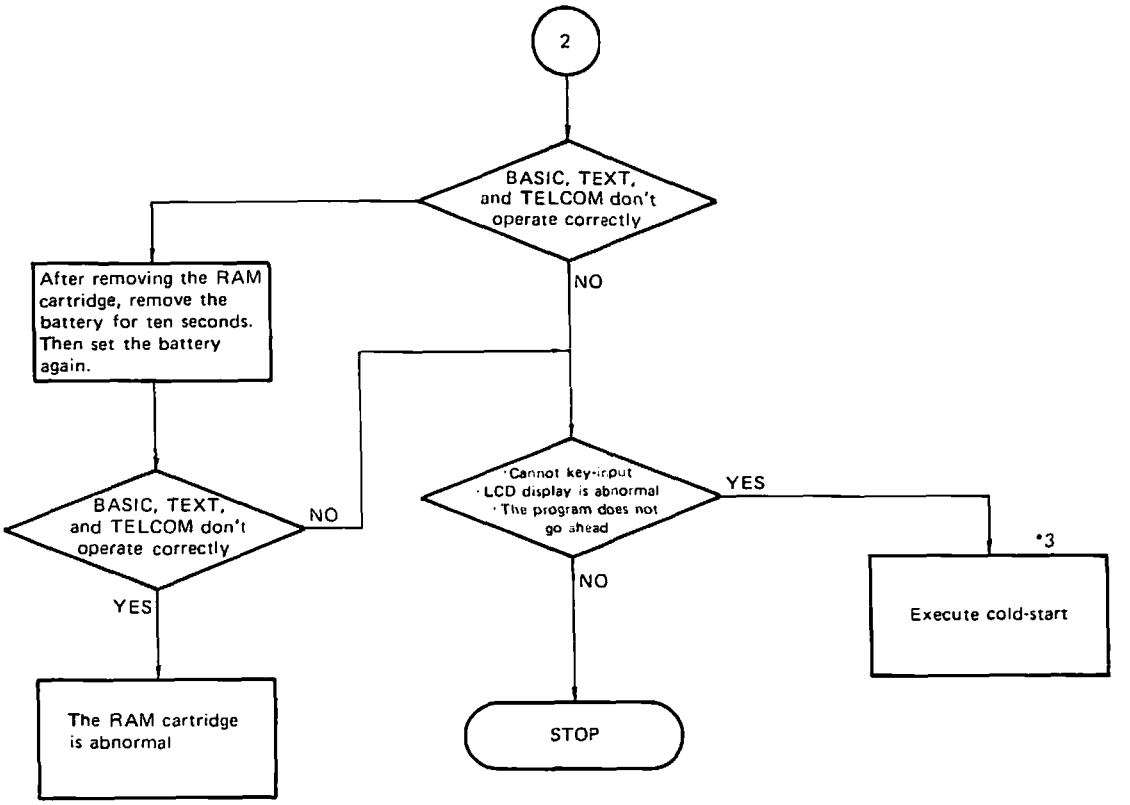
APPENDIX A
OPERATIONAL MISTAKES



*1: If bank #2 is not set, this operation is unneccessary.



2: If RAM cartridge isn't set, this operation is unneccessary.



*3: When executing cold-start, turn on the PROTECT switch of the PC-8201 and the one of the RAM cartridge.
But the program is Bank ≠1 is cleared.

APPENDIX B
IC REMOVAL

B-1 Necessary Equipment

(1) Solder Iron must be small (about 25 W); the tip should be thin.

(2) Solder
Use solder containing resin.

(3) Solder Remover

(4) IC puller
or cutting pliers (for board)
screwdriver (minus) (for socket)

B-2 ICs on Printed Circuit Board

(1) IC removal from circuit boards

a) Turn the board upside down. Remove the solder from IC pin holes with solder remover.

b) Gently pull the IC with a puller which fits the width and the number of pins. If you do not have a puller, pull carefully; be sure not to bend the pins with the pliers.

(2) Insertion

a) Insert the IC pins in their holes. turn board upside down. Use an electrically conductive mat under the PC-8201 when working on it.

b) Put a little solder on the iron.

c) Put the iron closely and heat. At once the solder melts. It is sucked in through the hole, and if it extends to the point of connecting, remove the iron.

– NOTE –

Do not allow excess spolder to pile up. The excess solder could cause electrical problems.

B-3 ICs with Sockets

(1) Removal from Socket

a) Gently pull the IC with a puller.
If you don't have a puller, use a screwdriver between the socket and the IC by prying up and down. Be careful not to bend the IC pins.

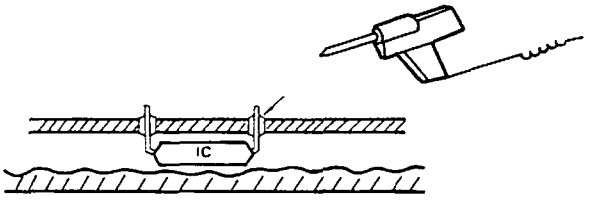
(2) Insertion in socket

a) Gently insert the IC.
If you don't have a puller, insert it after confirming that all pins have been inserted correctly.

B-4 Drawings of Insertion and Removal of IC

Removal

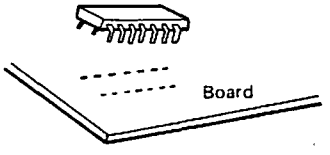
(1) Remove solder.



(2) Remove IC (with pliers or puller).

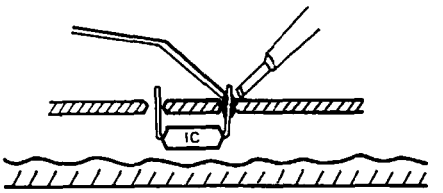
Installation

(1) Insert the IC pins in their holes.



(2) Melt some solder on tip of the iron.

(3) Attach some solder at the point of connection.



APPENDIX C
PARTS LIST

If you need to repair the PC-8201, change the unit parts.
Prepare the maintenance parts shown in Table 1.

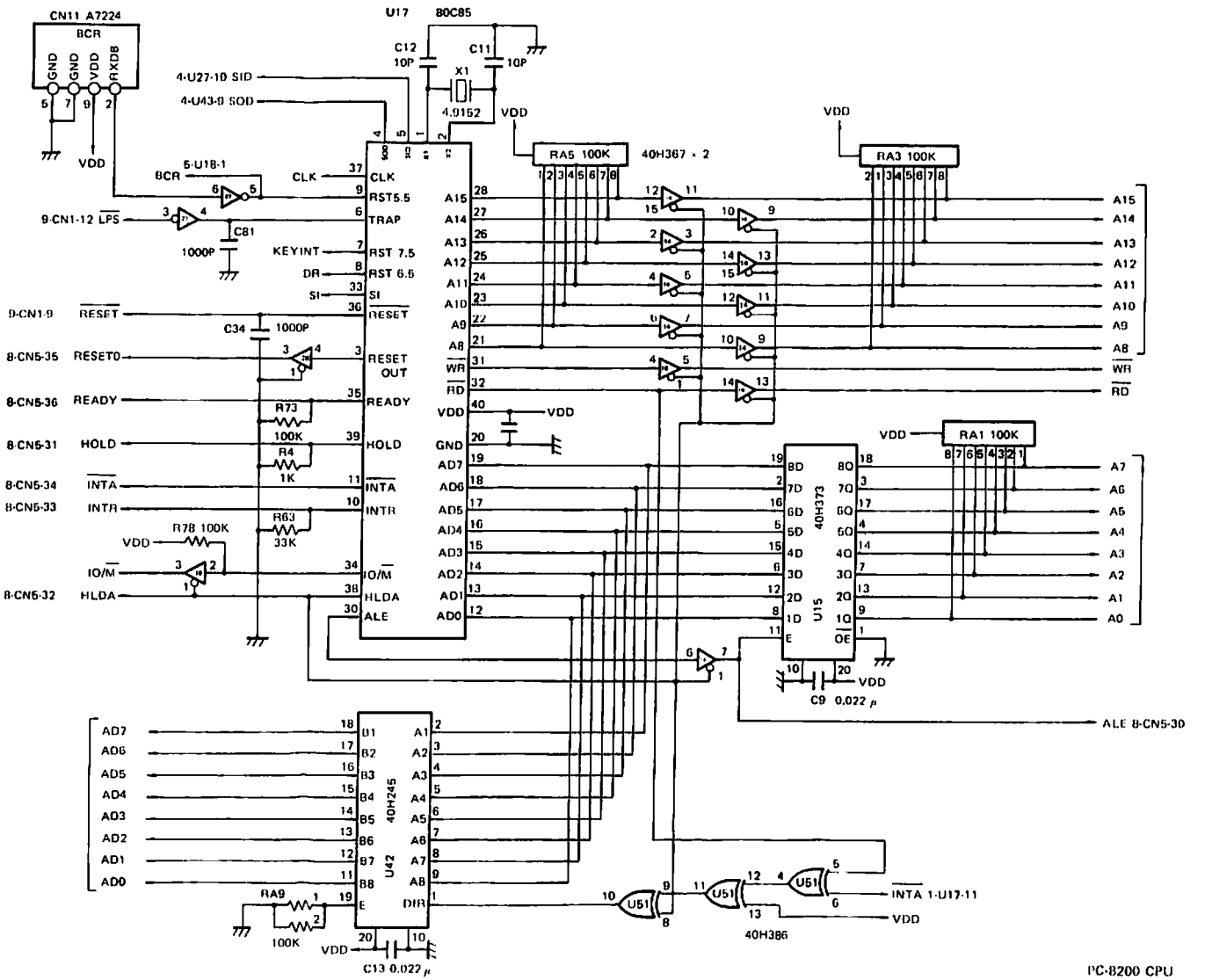
PARTS LIST

PART NAME	NOTE
MAIN PRINTED BOARD	WITH Ni-Cd BATTERY (Separate package)
POWER BOARD	
LCD UNIT	COMMON TO PC-8201 (JAPAN)
KEYBOARD UNIT	
PRINTER CONNECTOR BOARD	COMMON TO PC-8201 (JAPAN)
POWER BOARD CONNECTOR CABLE	COMMON TO PC-8201 (JAPAN)
PIEZO ELECTRO BUZZER (WITH CABLE)	COMMON TO PC-8201 (JAPAN)
BATTERY CASE UNIT	COMMON TO PC-8201 (JAPAN)
MASK ROM	
SPRING OF CARTRIDGE SLOT	COMMON TO PC-8201 (JAPAN)
TOP CASE	
BOTTOM CASE	COMMON TO PC-8201 (JAPAN)
Ni-Cd BATTERY	COMMON TO PC-8201 (JAPAN)
CARTRIDGE SLOT COVER	COMMON TO PC-8201 (JAPAN)
OPTION ROM/RAM COVER	COMMON TO PC-8201 (JAPAN)
FOOT RUBBER	COMMON TO PC-8201 (JAPAN)
PART OF CARTRIDGE SLOT	COMMON TO PC-8201 (JAPAN) (ADDITIONAL PART)
KEYBOARD SUPPORTING PART (UPPER)	COMMON TO PC-8201 (JAPAN) (ADDITIONAL PART)
KEYBOARD SUPPORTING PART (LOWER)	COMMON TO PC-8201 (JAPAN) (ADDITIONAL PART)
REAR SIDE CAP	COMMON TO PC-8201 (JAPAN) (ADDITIONAL PART)
SCREW KIT (6 items)	COMMON TO PC-8201 (JAPAN) (ADDITIONAL PART)
KEY SWITCH (TACT)	COMMON TO PC-8201 (JAPAN)
KEY SWITCH (CURSOR)	COMMON TO PC-8201 (JAPAN)
KEY SWITCH (PUSH)	COMMON TO PC-8201 (JAPAN)
KEY SWITCH (LOCK)	COMMON TO PC-8201 (JAPAN)
KEY TOP KIT (60 items)	

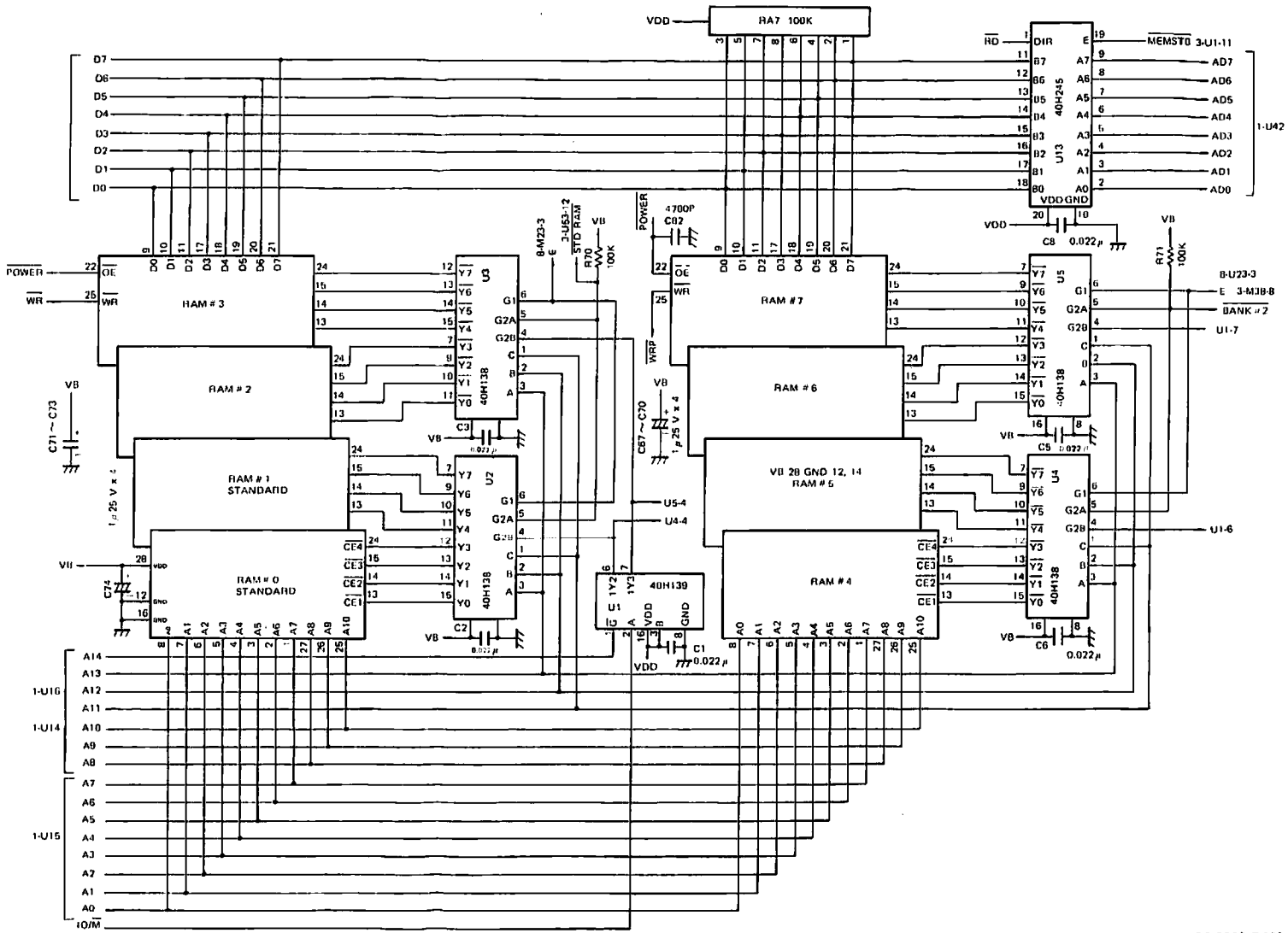
APPENDIX D
CIRCUIT DIAGRAM

PC-8201 Circuit

1. PC-8201 CPU Circuit
2. PC-8201 RAM Circuit
3. PC-8201 ROM Circuit
4. PC-8201 CMT Circuit
5. PC-8201 8155 Circuit
6. PC-8501 6402 Circuit
7. PC-8201 Keyboard Circuit
8. PC-8201 Connector Circuit
9. PC-8201 Power Source Unit Circuit

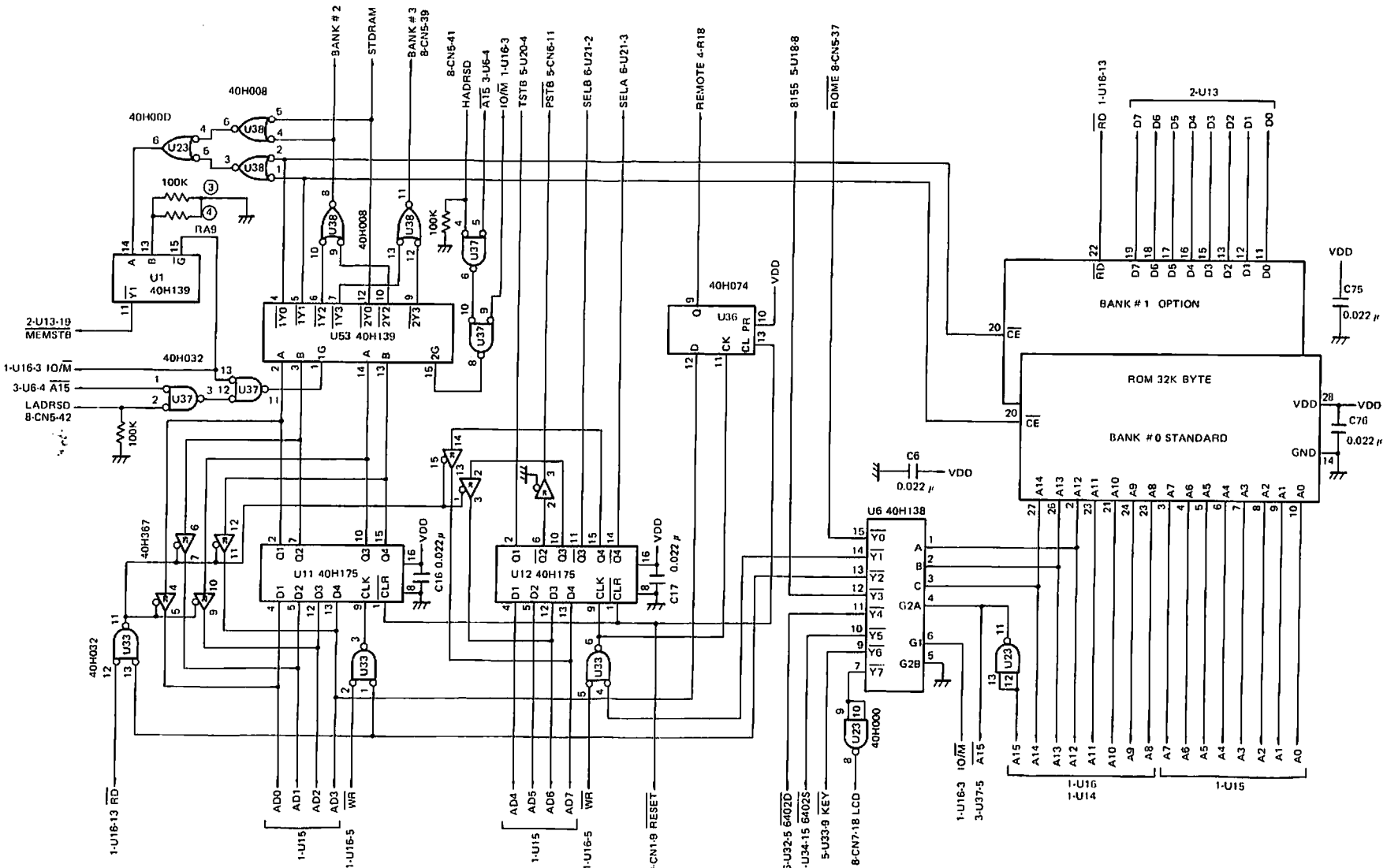

CN11 A7224
BCR
GND
GND
VDD
RXDB
U17 80C85
C12 10P
C11 10P
X1
4.9152
4-U27-10 SID
4-U43-8 SOD
VDD
5-U18-1
BCR
9-CN1-12 LPS
C81
1000P
CLK
RST5.5
TRAP
KEYINT
RST 7.5
RST 6.5
SI
RESET
C34 1000P
9-CN1-9 RESET
8-CN5-35 RESETO
RESET OUT
8-CN5-36 READY
R73 100K
8-CN5-31 HOLD
R4 1K
8-CN5-34 INTA
8-CN5-33 INTR
R63 33K
R78 100K
IO/M
8-CN5-32 HLDA
ALE
A15
A14
A13
A12
A11
A10
A9
A8
WR
RD
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
RA5 100K
40H367 × 2
RA3 100K
RA1 100K
40H373
U15
C9 0.022 μ
ALE 8-CN5-30
U42
40H245
RA9
100K
C13 0.022 μ
U51
40H386
INTA 1-U17-11

PC-8200 CPU

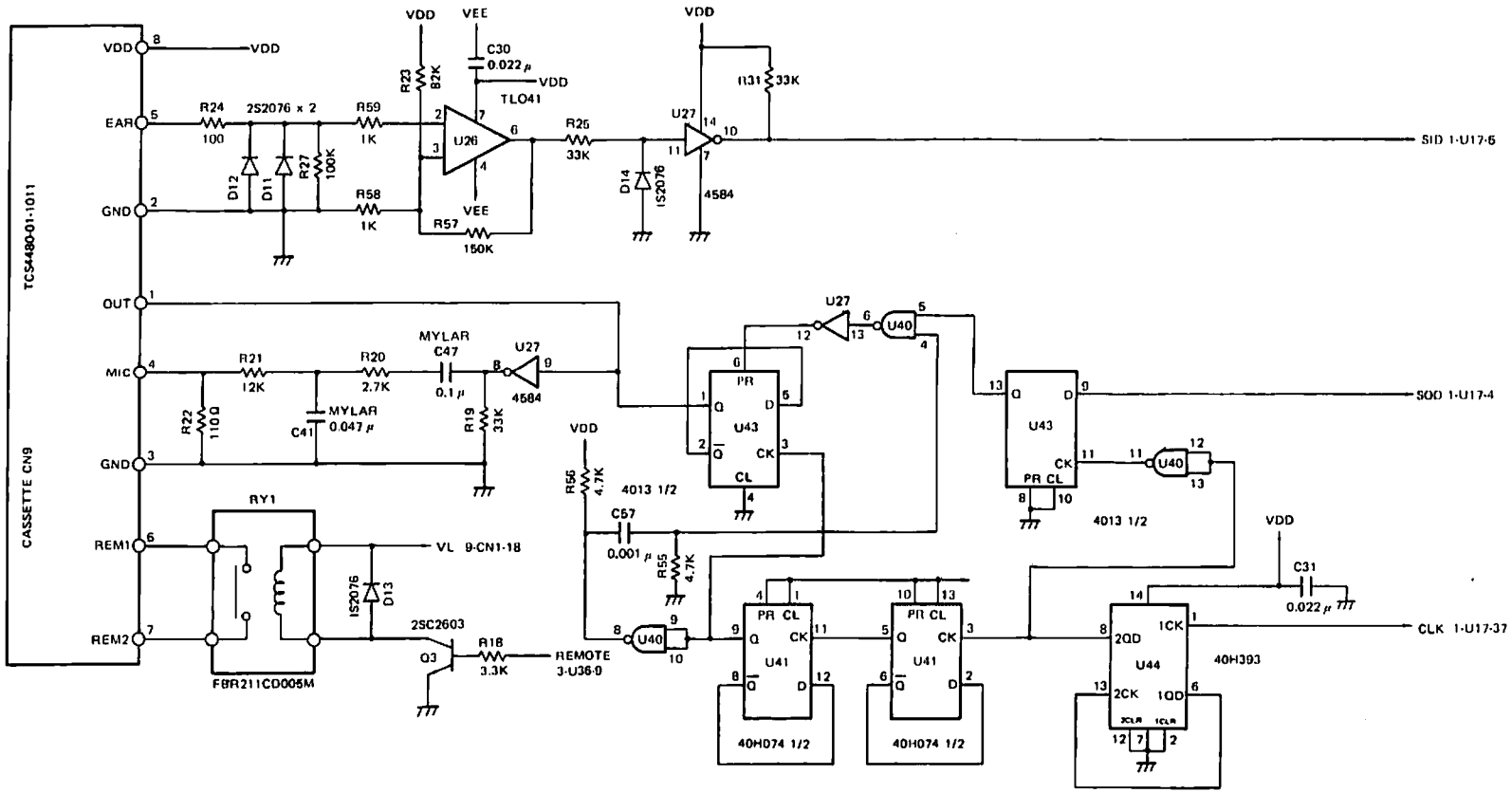


PC-8200 RAM

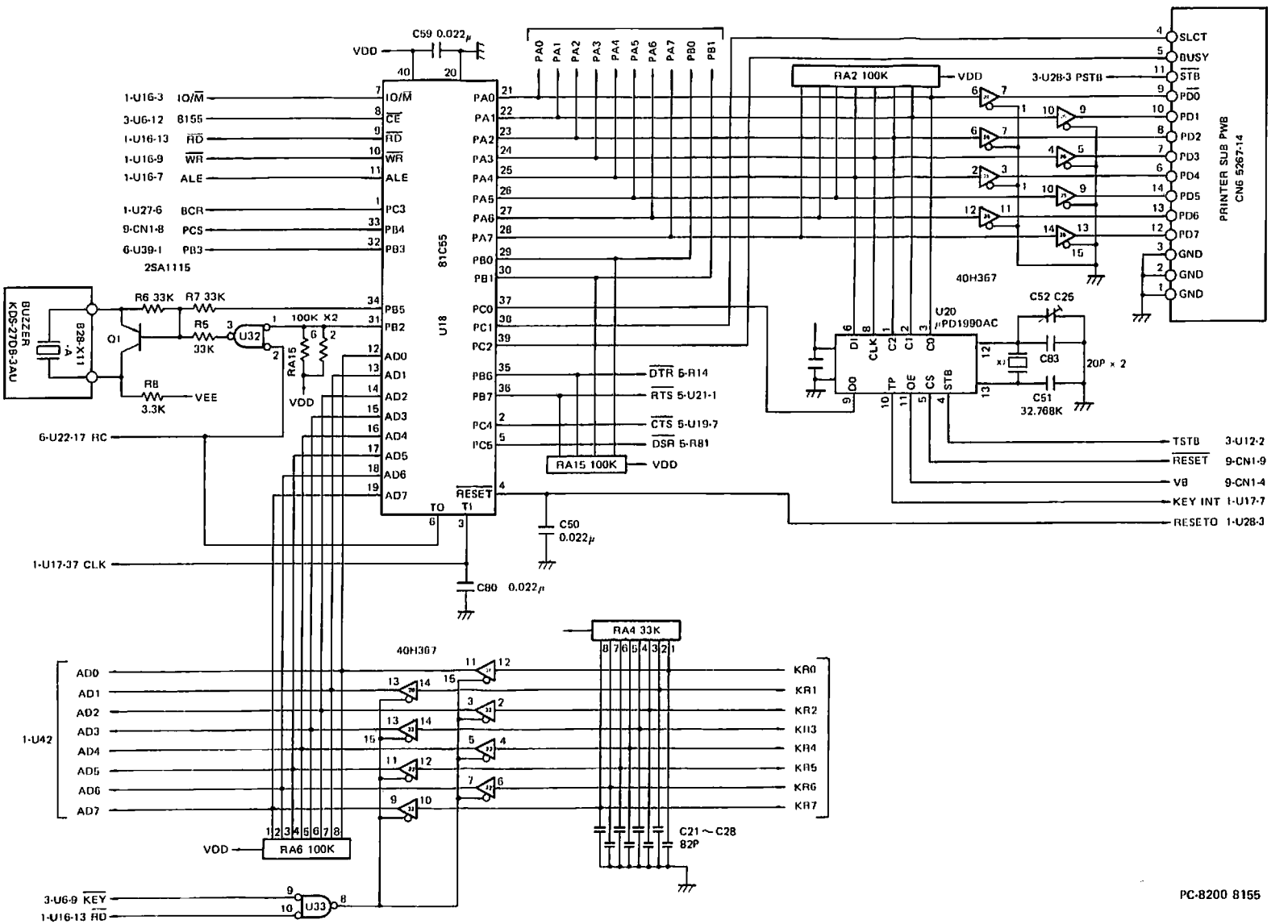
APX-D-5/APX-D-6 blank

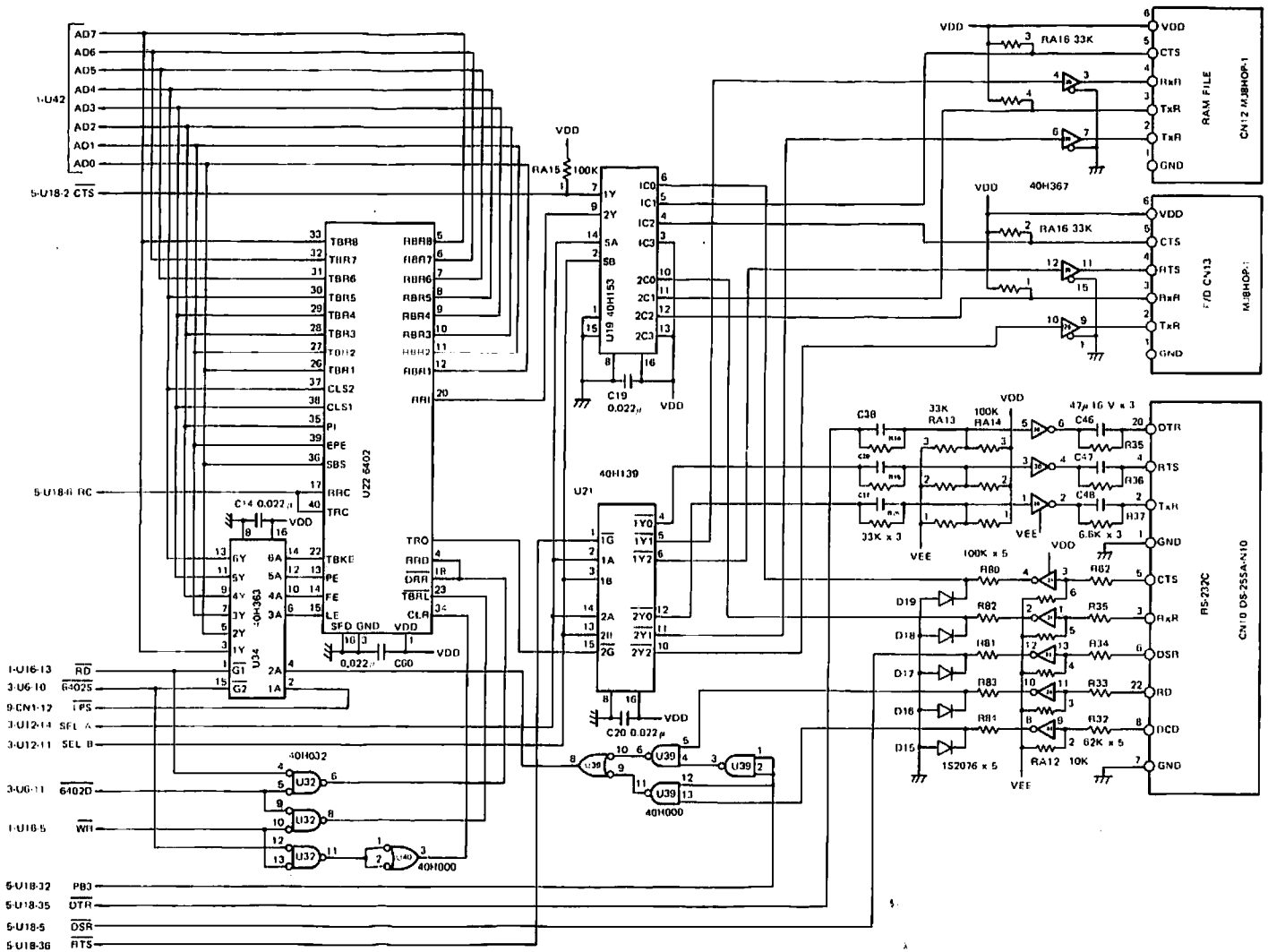

BANK # 2
STDRAM
BANK # 3
8-CN5-39
8-CN5-41
HADRSD
A15 3-U6-4
IO/M 1-U16-3
TSTB 5-U20-4
PSTB 5-CN6-11
SELB 6-U21-2
SELA 6-U21-3
REMOTE 4-R18
8155 5-U18-8
ROME 8-CN5-37
40H008
40H00D
100K
RA9
U1
40H139
2-U13-19
MEMSTB
U53 40H139
40H032
1-U16-3 IO/M
3-U6-4 A15
LADRSD
8-CN5-42
40H074
U36
VDD
2-U13
RD 1-U16-13
BANK # 1 OPTION
C75
0.022 μ
ROM 32K BYTE
BANK # 0 STANDARD
C76
GND
C6
U6 40H138
40H367
U11 40H175
U12 40H175
C16 0.022 μ
C17 0.022 μ
40H000
1-U16-13 RD
WR
RESET
6-U32-5 64020
6-U34-15 64025
5-U33-9 KEY
8-CN7-18 LCD
1-U16-3 IO/M
3-U37-5
1-U16
1-U14
1-U15

PC-8200 ROM

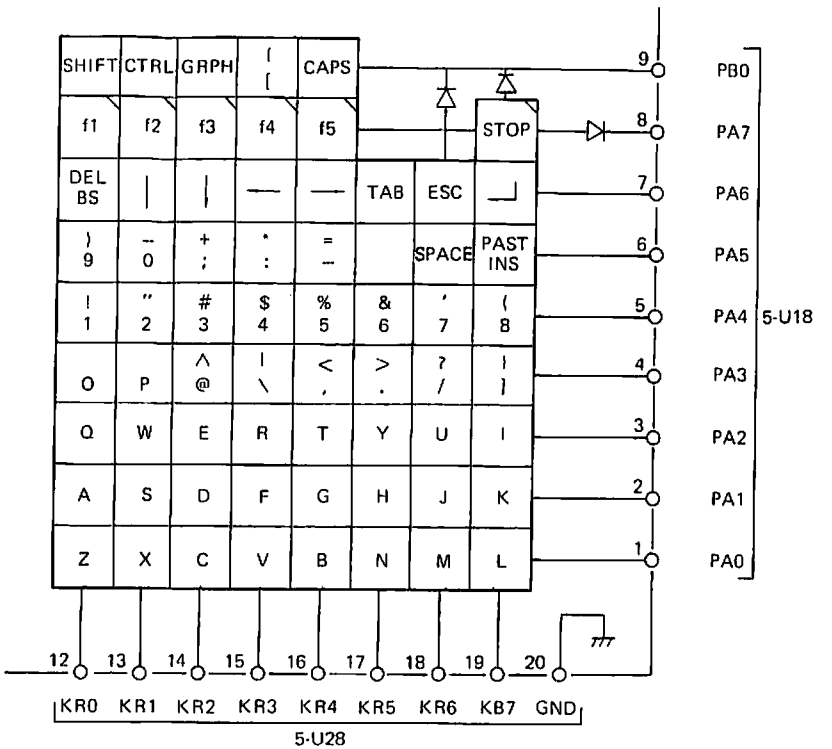

CASSETTE CN9
TCS4480-01-1011
VDD
VEE
C30
0.022 μ
TLO41
U26
R23
82K
R31
33K
R24
100
2S2076 x 2
R59
1K
R58
1K
R57
150K
R25
33K
U27
4584
D14
1S2076
SID 1-U17-6
EAR
GND
OUT
MIC
REM1
REM2
D12
D11
R27
100K
MYLAR
C47
0.1 μ
R21
12K
R20
2.7K
R22
110Ω
C41
MYLAR
0.047 μ
R19
33K
U40
U43
PR
CL
CK
4013 1/2
SOD 1-U17-4
R56
4.7K
C57
0.001 μ
R55
4.7K
RY1
FBR211CD005M
VL 9-CN1-18
1S2076
D13
2SC2603
Q3
R18
3.3K
REMOTE
3-U36-9
U41
PR CL
40H074 1/2
U44
40H393
1CK
2QD
1QD
2CK
C31
0.022 μ
CLK 1-U17-37

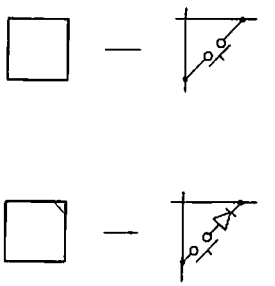
PC-8200 CMT

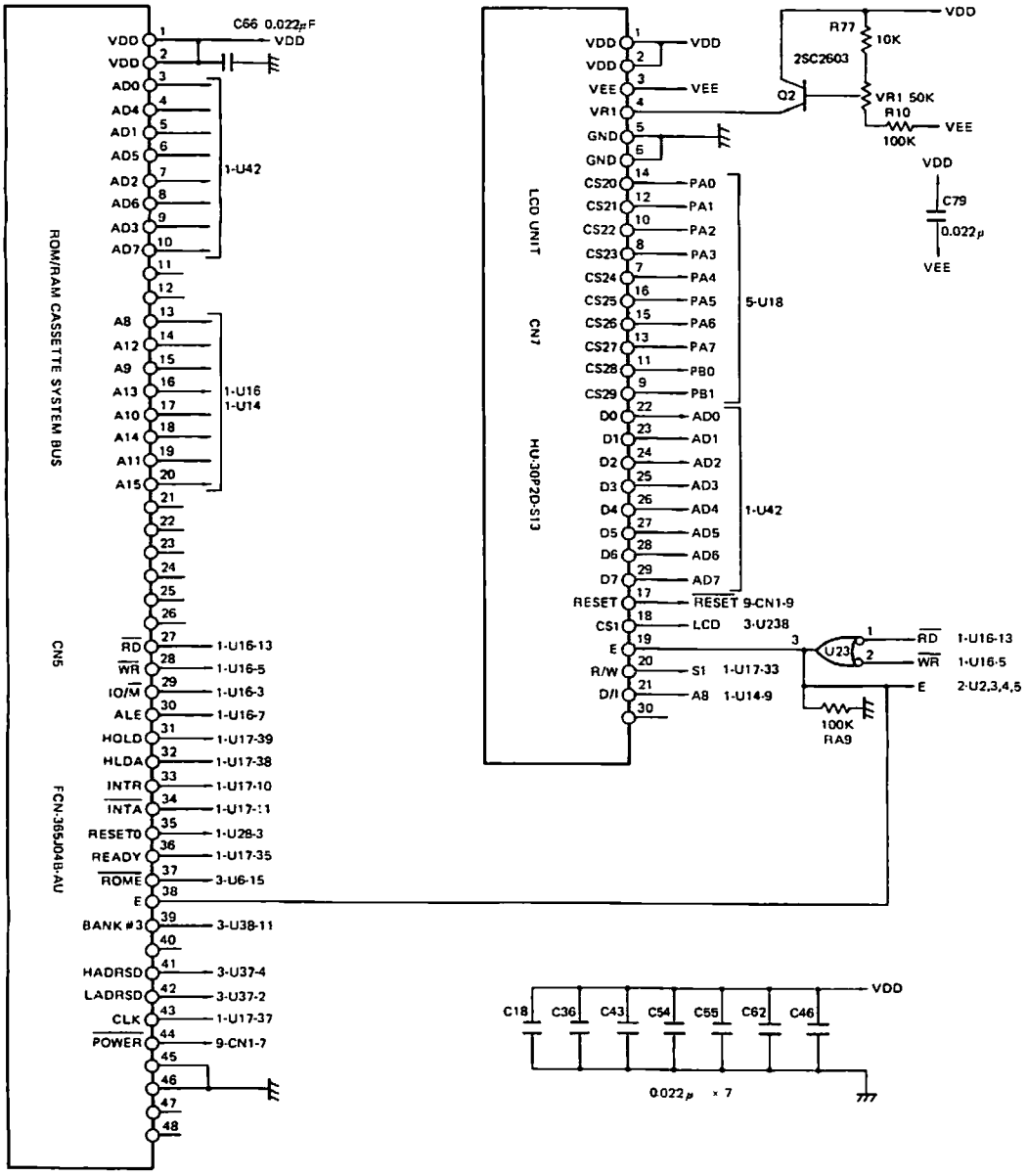

C59 0.022μ
VDD
81C55
U18
1-U16-3 IO/M
3-U6-12 8155
1-U16-13 RD
1-U16-9 WR
1-U16-7 ALE
1-U27-6 BCR
9-CN1-8 PCS
6-U39-1 PB3
2SA1115
R6 33K
R7 33K
R5 33K
R8 3.3K
VEE
Q1
U32
100K X2
RA15
VDD
6-U22-17 RC
1-U17-37 CLK
C50 0.022μ
C80 0.022μ
RESET
DTR 5-R14
RTS 5-U21-1
CTS 5-U19-7
DSR 5-R81
RA15 100K
RA2 100K
3-U28-3 PSTB
40H367
U20 μPD1990AC
C52 C25
C83 20P × 2
C51 32.768K
PRINTER SUB PWB CN6 5267-14
SLCT
BUSY
STB
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
GND
TSTB 3-U12-2
RESET 9-CN1-9
VB 9-CN1-4
KEY INT 1-U17-7
RESETO 1-U28-3
RA4 33K
RA6 100K
1-U42
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
KR0
KR1
KR2
KR3
KR4
KR5
KR6
KR7
C21 ~ C28 82P
3-U6-9 KEY
1-U16-13 RD
U33
PC-8200 8155


AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
5-U18-2 CTS
5-U18-6 RC
1-U16-13 RD
3-U6-10 64025
9-CN1-12 IPS
3-U12-14 SEL A
3-U12-11 SEL B
3-U6-11 6402D
1-U16-5 WR
5-U18-32 PB3
5-U18-35 OTR
5-U18-5 DSR
5-U18-36 RTS
U22 6402
TBR8
TBR7
TBR6
TBR5
TBR4
TBR3
TBR2
TBR1
CLS2
CLS1
PI
EPE
SBS
RRC
TRC
TBRE
PE
FE
LE
SFD GND
VDD
RBR8
RBR7
RBR6
RBR5
RBR4
RBR3
RBR2
RBR1
RRI
TRO
DRR
TBRL
CLR
C14 0.022µ
C60 0.022µ
U34 40H363
U32 40H032
40H000
RA15 100K
U19 40H153
C19 0.022µ
U21 40H139
C20 0.022µ
U39 40H000
40H367
RA16 33K
RAM FILE
CN12 M.BHOP-1
F/D CN13
M.BHOP-1
C38
33K RA13
100K RA14
47µ 16 V x 3
C46
C47
C48
R35
R36
R37
33K x 3
6.8K x 3
100K x 5
R80
R82
R81
R83
R84
R32
R33
R34
62K x 5
RA12 10K
D19
D18
D17
D16
D15
1S2076 x 5
CN10 DS-25SA-N10
RS-232C
OTR
RTS
TxR
GND
CTS
RxR
DSR
RD
DCD
VEE

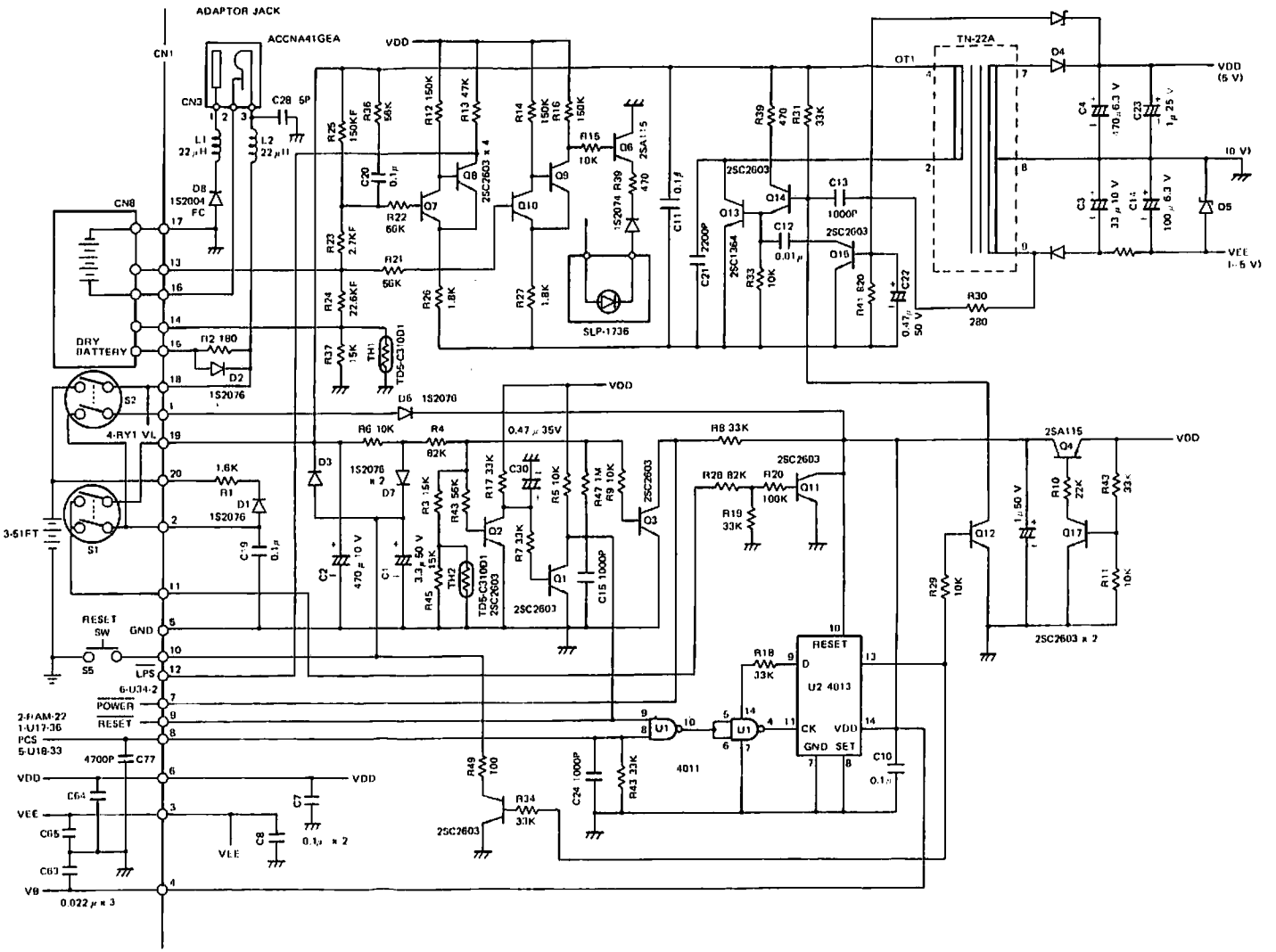
PC-8200 6402


SHIFT
CTRL
GRPH
CAPS
f1
f2
f3
f4
f5
STOP
DEL BS
TAB
ESC
SPACE
PAST INS
9
8
7
6
5
4
3
2
1
PB0
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
5-U18
12
13
14
15
16
17
18
19
20
KR0
KR1
KR2
KR3
KR4
KR5
KR6
KB7
GND
5-U28





PC-8200 CONNECTOR



PC-8200 POWER SUPPLY

APPENDIX E
LSI DATA SHEET

MSM80C85A AS/RS

Single Chip 8-Bit CMOS Microprocessor

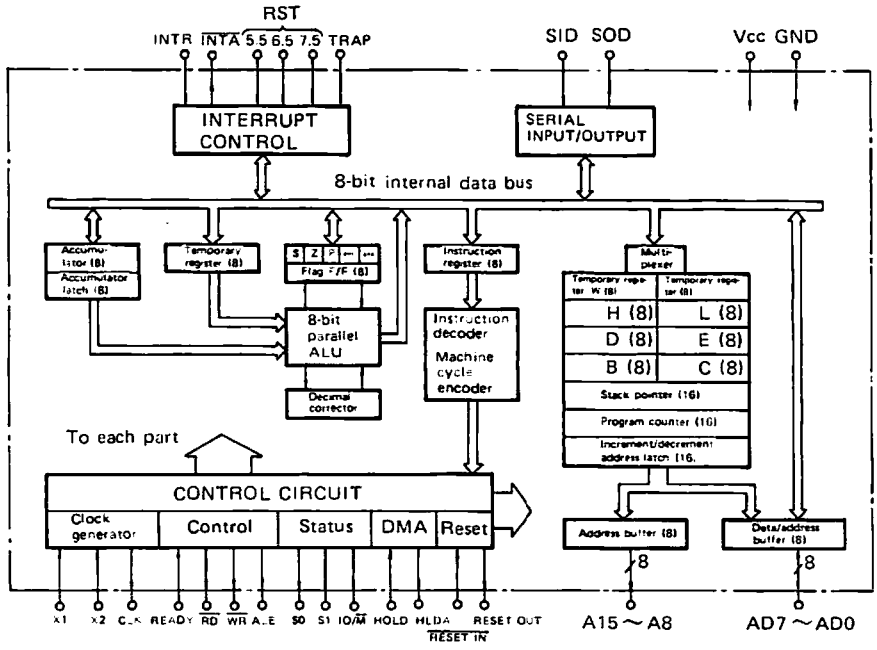
General

The MSM80C85A is an 8-bit, 1-chip parallel processing CPU employing silicon-gate CMOS technology. The MSM80C85A, compatible with the MSM8085A, has almost the same processing capabilities and low power dissipation as compared with the MSM8085A; promising high-performance system configuration.

Features

- High speed and low-power dissipation enabled by use of silicon-gate CMOS technologies
- Single power supply of 3 V to 6 V
- Compatibility with MSM8085A
- Instruction cycle: 1.3 μs on Vcc = 5 V
- Built-in clock oscillator
- For vectored interrupts (One nonmaskable)
- Built-in serial input/output ports (One input, one output)
- Direct addressing of 64K Byte storage
- Compatible with Intel 8085A

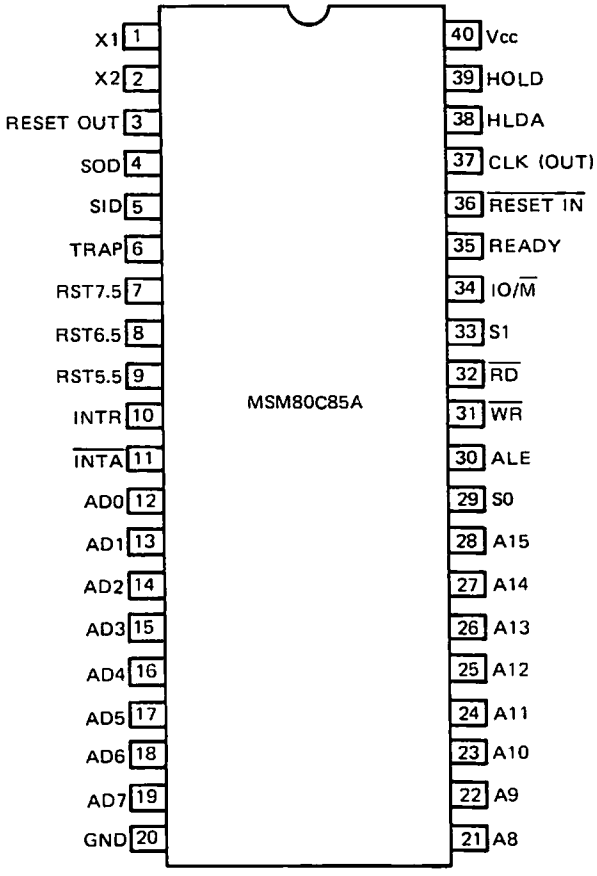
Circuit Configuration



(These specifications are subject to change without notice.)

Pin Connections

(Top View) 40 Lead Plastic DIP



Description of Pins Functions

Pin symbol	Name	Input/ Output	Functions
A8 ~ A15	Address buses	Output	Upper eight bits of storage address or eight bits of I/O address; placed in high-impedance state at HOLD and HALT modes.
AD0 ~ AD7	Bilateral address & data buses	Input/ Output	Lower eight bits of storage address or I/O address appear on these buses at the first clock cycle. They serve as data buses during the second and third clock cycles. Placed into high-impedance state at HOLD and HALT modes.
ALE	Address latch enabling output	Output	Generated during the first clock cycle; used by peripherals to latch address. Trailing edge permits setup time and hold time required to latch address data. ALE signal may also be used to strobe status data.
S0, S1	Status output	Output	Bus status S1 S0 HALT 0 0 WRITE 0 1 READ 1 0 FETCH 1 1 S1 code can be used as early indicution of R/W status.
$\overline{RD}$	Read Data	Output	Used to select storage or I/O address for read or to show that data bus should be used in data transfer. Placed in high-impedance state at HOLD and HALT modes.
$\overline{WR}$	Write data	Output	Enable data on data bus to be written into selected storage or I/O address. Data is written at trailing edge of WR. Placed in high-impedance state at HOLD and HALT modes.
RST5.5 RST6.5 RST7.5	Restart interrupt request (input)	Input	These three input signals have the same timing as INTR signal except that they are capable of internal and automatic insertion of the RESTART signal. RST7.5 has highest priority and RST5.5 the lowest. This group of interrupt signals have priority over INTR.
TRAP	Trap interrupt input	Input	Trap interrupt is a restart interrupt signal that cannot be masked, and can be accepted at the same timing as INTR. The trap interrupt input signal has highest priority and is not masked or enabled.
$\overline{RESET}$ $\overline{IN}$	Reset input	Input	This reset signal, at least three clock pulses of which should be input, resets program counter at 0 and resets interrupt enable and HLDA. Not affected by flags or any register except the instruction register. RESET IN continues to be asserted as long as it is low.
RESET OUT	Reset output	Output	RESET OUT can be used to reset system, indicating that the CPU is being reset. RESET OUT must be synchronized with processor clock signal.

Pin symbol	Name	Input/ Output	Functions
X1. X2	Clock inputs	Input	These two pins serve to connect external crystal oscillator for the purpose of generating clock signals internally. Pin X1 can also receive externally generated clock signals.
CLK	Clock output	Output	This clock signal, used as clock output, is generated by crystal oscillator connected externally to CPU.
IO/$\overline{M}$	Data transfer control output	Output	Indicates whether data transfer is to memory or I/O unit. Put into high-impedance state at HOLD and HALT modes.
READY	Ready signal	Input	Indicates that storage or peripheral is ready for data transfer when READY is high. When READY is low. CPU will not complete data transfer cycle until READY become high again. READY should be given sufficient set-up time and hold time.
HOLD	Hold request signal	Input	At HOLD, CPU relinquishes bus control immediately upon completion of the current machine cycle. CPU resumes bus control after released from HOLD. CPU places address bus, data bus, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ in high-impedance state upon acknowledging HOLD.
HLDA	Hold response signal	Output	Acknowledges HOLD request; indicates that CPU will relinquish bus control at the next clock cycle. Upon completion of HOLD, HLDA goes low. At the half clock cycle following the disasserted HLDA, CPU resumes bus control.
INTR	Interrupt request signal	Input	Used as general-purpose interrupt request. INTR executes sampling only at the last clock cycle of instruction. When interrupt is received, INTR stops the program counter and asserts INTA. RESTART or CALL signal can be inserted to m make an interruption in this cycle so as to make a jump to service rutines. Interrupt request is inhibited by receivt of RESET or interrupt. INTR is software maskable.
$\overline{INTA}$	Interrupt reception control signal	Output	Used instead of $\overline{RD}$ at the same time as $\overline{RD}$ signal in instruction cycle after INTR received.
SID	Serial data	Input	Serial data input pin. Data on this line is stored in accumulator bit 7 when RIM instruction executed.
SOD	Serial data output	Output	Serial data output pin. Data is output using SIM instruction.

Functions

- Outline

  The MSM80C85A uses a multiplexed data and address bus. The upper eight bits of an address are output to the address bus and the lower eight bits to the address/data bus. The lower eight-bit addresses can be output only in the first state in each machine cycle. They must be held in an external latch by simultaneously using ALE. The address/data bus serves as a bilateral data bus the same way as in the MSM8080A.
  Data is transferred on the bilateral data bus. The CPU outputs $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ signals for bus control signal and $\overline{INTA}$ for interrupt reception. The CPU receives HOLD, READY, and interrupt signals synchronized with the clock.
  For serial transmission of data, serial-data input SID and serial-data output SOD, are available. Three maskable restart interrupts and one unmaskable TRAP interrupt are available in addition to those of the MSM8080A.

- Status data

  Status data is a signal that indicates the bus cycle status. This signal is output from pins S0 or S1 and held until completion of the cycle. In contrast to the MSM80C85A, status data in the MSM8080A are output from data bus at the start of each machine cycle. Bus status are given as follows:

	S1	S0
HALT	0	0
WRITE	0	1
READ	1	0
FETCH	1	1

- Interrupts and serial I/O

  The MSM80C85A is provided with five interrupt input lines: INTR, RST5.5, RST6.5, RST7.5, and TRAP. INTR functions the same as the MSM8080A INT. RST input lines 5.5, 6.5, and 7.5 are all maskable restart interrupts. TRAP is an unmaskable restart interrupt. Restart interrupt priority is determined in terms of the restart address, how to sense interrupt, and internal priority. TRAP has highest priority, followed by RST7.5, RST6.5, RST5.5 and INTR.
  Note that this preferential order is not taken into account for routines already running even if higher-preference interruption is made to them. If RST5.5 is asserted during an RST7.5 routine, execution of RST7.5 is suspended. RST6.5, RST5.5, and INT should all be asserted until their interrupt requests are acknowledged. While RST7.5 may be input in the form of pulse because its request is detected at its leading edge to be set. A request thus set is held until it is satisfied or SIM or RESET instructions release the request state. An RST7.5 request can be set even if masked; interruption is inhibited.
  TRAP is detected at its leading edge and should be asserted until the request is accepted. Before TRAP can be accepted a second time, it must first be disasserted.

then reasserted. Serial I/O is controlled by the RIM and SIM instruction. SID is read in by the RIM instruction and the SIM instruction sets SOD data.

Name	Restart address (hex)	Where sensed
TRAP	24_{16}	Level and edge
RST7.5	$3C_{16}$	Edge
RST6.5	34_{16}	Level
RST5.5	$2C_{16}$	Level

- Basic timing
  The MSM80C85A uses a multiplexed data and address bus. ALE is used to latch the lower eight bits of the address on the data bus. Figure 1 shows three basic cycles of the instruction fetch cycle, the storage content read cycle, and the I/O write-in cycle. At the I/O read and write cycles, the upper and lower eight bits of the address become equal. If slower storage or I/O is used in the MSM80C85A, TWAIT status can be inserted using the READY signal, the same as with the MSM8080A.

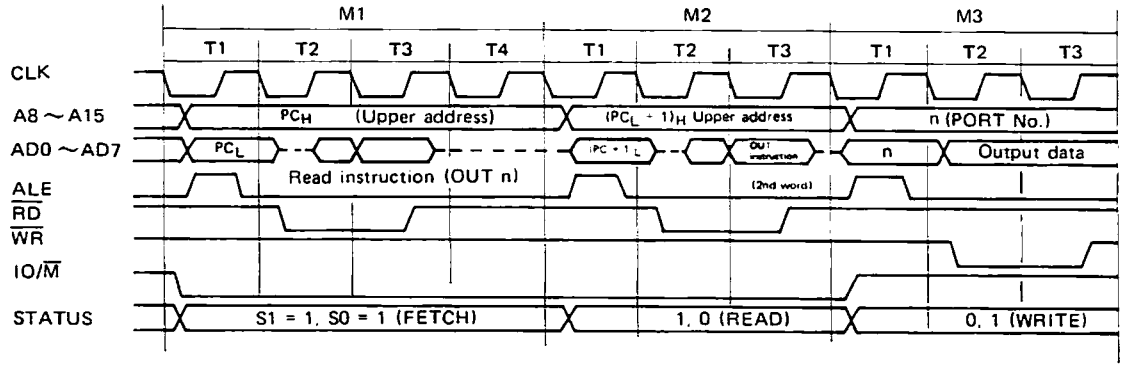
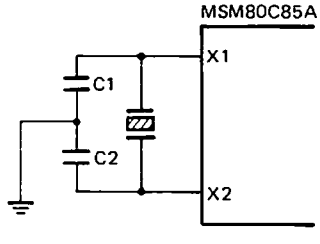


Figure 1 Basic Timing Chart for Instructions

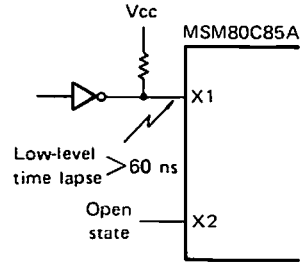
- Driving circuits for inputs X1 and X2
  Inputs X1 and X2 of the MSM80C85A can be driven either by a crystal oscillator or external clock pulse.

  Recommended circuits for oscillation



C1 = C2 = 50 pF when input frequency is 4 to 6 MHz.

C1 = C2 = 100 pF when input frequency is 1 to 4 MHz.



Input frequency is 1 to 6 MHz (external clock pulse)

List of Machine Instructions

Classification	Instruction symbol		Instruction code D7 D6	D5 D4 D3	D2 D1 D0	Hexadecimal representation	Required number of states	Number of bytes	Number of cycle	Functions
Data transfer instructions	MOV	r1, r2	0 1	D D D	S S S		4	1	1	(r1) — (r2)
	MOV	M, r	0 1	1 1 0	S S S	7	7	1	2	(M) — (r) where M = (H) (L)
	MOV	r, M	0 1	D D D	1 1 0	7	7	1	2	(r) — (M) where M = (H) (L)
	MVI	r, n	0 0	D D D < B2 >	1 1 0	7	7	2	2	(r) — n
	MVI	M, n	0 0	1 1 0 < B2 >	1 1 0	3 6	10	2	3	(M) — n where M = (H) (L)
	LXI	B, m	0 0	0 0 0 < B2 > < B3 >	0 0 1	0 1	10	3	3	(C) — <B2> (B) — <B3> where m = <B3><B2>
	LXI	D, m	0 0	0 1 0 < B2 > < B3 >	0 0 1	1 1	10	3	3	(E) — <B2> (D) — <B3> where m = <B3><B2>
	LXI	H, m	0 0	1 0 0 < B2 > < B3 >	0 0 1	2 1	10	3	3	(L) — <B2> (H) — <B3> where m = <B3><B2>
	LXI	SP, m	0 0	1 1 0 < B2 > < B3 >	0 0 1	3 1	10	3	3	(SP) — m
	SPHL		1 1	1 1 1	0 0 1	F 9	6	1	1	(SP) — (H) (L)
	STAX	B	0 0	0 0 0	0 1 0	0 2	7	1	2	((B) (C)) — (A)
	STAX	D	0 0	0 1 0	0 1 0	1 2	7	1	2	((B) (C)) — (A)
	LDAX	B	0 0	0 0 1	0 1 0	0 A	7	1	2	(A) — ((B) (C))
	LDAX	D	0 0	0 1 1	0 1 0	1 A	7	1	2	(A) — ((D) (E))
	STA	m	0 0	1 1 0 < B2 > < B3 >	0 1 0	3 2	13	3	4	(m) — (A)
	LDA	m	0 0	1 1 1 < B2 > < B3 >	0 1 0	3 A	13	3	4	(A) — (m)
	SHLD	m	0 0	1 0 0 < B2 > < B3 >	0 1 0	2 2	16	3	5	(m) — (L) (m + 1) — (H)
	LHLD	m	0 0	1 0 1 < B2 > < B3 >	0 1 0	2 A	16	3	5	(L) — (m) (H) — (m + 1)
	XCHG		1 1	1 0 1	0 1 1	E B	4	1	1	(H) (L) — (D) (E)
	XTHL		1 1	1 0 0	0 1 1	E 3	16	1	5	(H) (L) — ((SP) + 1) ((SP))
Addition and subtraction/Boolean operation/comparison instructions	ADD	r	1 0	0 0 0	S S S		4	1	1	(A) — (A) + (r)
	ADD	M	1 0	0 0 0	1 1 0	8 6	7	1	2	(A) — (A) + (M) where M = (H) (L)
	ADI	n	1 1	0 0 0 < B2 >	1 1 0	C 6	7	2	2	(A) — (A) + n
	ADC	r	1 0	0 0 1	S S S		4	1	1	(A) — (A) + (r) + (CY2) where
	ADC	M	1 0	0 0 1	1 1 0	8 E	7	1	2	(A) — (A) + (M) + (CY2) M = (H) (L)
	ACI	n	1 1	0 0 1 < B2 >	1 1 0	C E	7	2	2	(A) — (A) + n + (CY2)
	DAD	B	0 0	0 0 1	0 0 1	0 9	10	1	3	(H) (L) — (H) (L) + (B) (C)
	DAD	D	0 0	0 1 1	0 0 1	1 9	10	1	3	(H) (L) — (H) (L) + (D) (E)
	DAD	H	0 0	1 0 1	0 0 1	2 9	10	1	3	(H) (L) — (H) (L) + (H) (L)
	DAD	SP	0 0	1 1 1	0 0 1	3 9	10	1	3	(H) (L) — (H) (L) + (SP)
	SUB	r	1 0	0 1 0	S S S		4	1	1	(A) — (A) − (r)
	SUB	M	1 0	0 1 0	1 1 0	9 6	7	1	2	(A) — (A) − (M) where M = (H) (L)
	SUI	n	1 1	0 1 0 < B2 >	1 1 0	D 6	7	2	2	(A) — (A) − n
	SBB	r	1 0	0 1 1	S S S		4	1	1	(A) — (A) − (r) − (CY2) where
	SBB	M	1 0	0 1 1	1 1 0	9 E	7	1	2	(A) — (A) − (M) − (CY2) M = (H) (L)
	SBI	n	1 1	0 1 1 < B2 >	1 1 0	D E	7	2	2	(A) — (A) − n − (CY2)
	ANA	r	1 0	1 0 0	S S S		4	1	1	(A) — (A) ∧ (r)
	ANA	M	1 0	1 0 0	1 1 0	A 6	7	1	2	(A) — (A) ∧ (M) where M = (H) (L)
	ANI	n	1 1	1 0 0 < B2 >	1 1 0	E 6	7	2	2	(A) — (A) ∧ n

List of Machine Instructions (Cont)

Classification	Instruction symbol	D7 D6	D5 D4 D3	D2 D1 D0	Hexadecimal representation	Required number of states	Number of bytes	Number of cycle	Functions
Addition and subtraction logical operation/comparison instruction	XRA r	1 0	1 0 1	S S S		4	1	1	(A) ← (A) ∀ (r)
	XRA M	1 0	1 0 1	1 1 0	A E	7	1	2	(A) ← (A) ∀ (M) where M = (H) (L)
	XRI n	1 1	1 0 1	1 1 0	E E	7	2	2	(A) ← (A) ∀ n
			< B2 >						
	ORA r	1 0	1 1 0	S S S		4	1	1	(A) ← (A) ∨ (r)
	ORA M	1 0	1 1 0	1 1 0	B 6	7	1	2	(A) ← (A) ∨ (M) where M = (H) (L)
	ORI n	1 1	1 1 0	1 1 0	F 6	7	2	2	(A) ← (A) ∨ n
			< B2 >						
	CMP r	1 0	1 1 1	S S S		4	1	1	(A) − (r) Two numbers
	CMP M	1 0	1 1 1	1 1 0	B E	7	1	2	(A) − (M) are compared M = (H) (L)
	CPI n	1 1	1 1 1	1 1 0	F E	7	2	2	(A) − n to each other, assuming that
			< B2 >						
Instructions for increasing and decreasing register content	INR r	0 0	D D D	1 0 0		4	1	1	(r) ← (r) + 1
	INR M	0 0	1 1 0	1 0 0	3 4	10	1	3	(M) ← (M) + 1 where M = (H) (L)
	DCR r	0 0	D D D	1 0 1		4	1	1	(r) ← (r) − 1
	DCR M	0 0	1 1 0	1 0 1	3 5	10	1	3	(M) ← (M) − 1 where M = (H) (L)
	INX B	0 0	0 0 0	0 1 1	0 3	6	1	1	(B) (C) ← (B) (C) + 1
	INX D	0 0	0 1 0	0 1 1	1 3	6	1	1	(D) (E) ← (D) (E) + 1
	INX H	0 0	1 0 0	0 1 1	2 3	6	1	1	(H) (L) ← (H) (L) + 1
	INX SP	0 0	1 1 0	0 1 1	3 3	6	1	1	(SP) ← (SP) + 1
	DCX B	0 0	0 0 1	0 1 1	0 B	6	1	1	(B) (C) ← (B) (C) − 1
	DCX D	0 0	0 1 1	0 1 1	1 B	6	1	1	(D) (E) ← (D) (E) − 1
	DCX H	0 0	1 0 1	0 1 1	2 B	6	1	1	(H) (L) ← (H) (L) − 1
	DCX SP	0 0	1 1 1	0 1 1	3 B	6	1	1	(SP) ← (SP) − 1
Accumulator rotation shift instruction	RLC	0 0	0 0 0	1 1 1	0 7	4	1	1	Left shift CY2 ← A7 A6 ····· A1 A0 ← A7
	RRC	0 0	0 0 1	1 1 1	0 F	4	1	1	Right shift CY2 → A7 A6 ····· A1 A0 → A0
	RAL	0 0	0 1 0	1 1 1	1 7	4	1	1	Left shift CY2 ← A7 A6 ····· A1 A0 ← CY2
	RAR	0 0	0 1 1	1 1 1	1 F	4	1	1	Right shift CY2 → A7 A6 ····· A1 A1 → CY2
Accumulator correction instructions	CMA	0 0	1 0 1	1 1 1	2 F	4	1	1	A ← $\overline{(A)}$
	DAA	0 0	1 0 0	1 1 1	2 7	4	1	1	Binary-coded decimal adjust of binary sum in accumulator
Carry setting instruction	STC	0 0	1 1 0	1 1 1	3 7	4	1	1	(CY2) ← 1
	CMC	0 0	1 1 1	1 1 1	3 F	4	1	1	(CY2) ← $\overline{(CY2)}$
Jump instruction	JMP m	1 1	0 0 0	0 1 1	C 3	10	3	3	(PC) ← m
			< B2 >						
			< B3 >						
	PCHL	1 1	1 0 1	0 0 1	E 9	6	1	1	(PC) ← (H) (L)
	JC m	1 1	0 1 1	0 1 0	D A	10/7	3	3/2	(CY2) = 1
			< B2 >						
			< B3 >						
	JNC m	1 1	0 1 0	0 1 0	D 2	10/7	3	3/2	(CY2) = 0 If condition true, (PC) ← m
			< B2 >						
			< B3 >						
	JZ m	1 1	0 0 1	0 1 0	C A	10/7	3	3/2	(Z) = 1
			< B2 >						
			< B3 >						
	JNZ m	1 1	0 0 0	0 1 0	C 2	10/7	3	3/2	(Z) = 0
			< B2 >						
			< B3 >						
	JP m	1 1	1 1 0	0 1 0	F 2	10/7	3	3/2	(S) = 0 If condition false, (PC) ← (PC) + 3
			< B2 >						
			< B3 >						
	JM m	1 1	1 1 1	0 1 0	F A	10/7	3	3/2	(S) = 1
			< B2 >						
			< B3 >						
	JPE m	1 1	1 0 1	0 1 0	E A	10/7	3	3/2	(P) = 1
			< B2 >						
			< B3 >						
	JPO m	1 1	1 0 0	0 1 0	E 2	10/7	3	3/2	(P) = 0
			< B2 >						
			< B3 >						

List of Machine Instructions (Cont)

Classification	Instruction symbol		Instruction code D7 D6	D5 D4 D3	D2 D1 D0	Hexadecimal representation	Required number of states	Number of bytes	Number of cycle	Functions
Subroutine call instruction	CALL	m	1 1	0 0 1 <B2> <B3>	1 0 1	C D	18	3	5	((SP) − 1) ((SP) − 2) ← (PC) + 3, (PC) ← m (SP)←(SP) − 2
	RST	n	1 1	A A A	1 1 1		12	1	3	((SP) − 1) ((SP) − 2) ← (PC) + 1, (PC) ← n × 8, (SP) ← (SP) − 2 where 0≤n≤7
	CC	m	1 1	0 1 1 <B2> <B3>	1 0 0	D C	18/9	3	5/2	(CY2) = 1
	CNC	m	1 1	0 1 0 <B2> <B3>	1 0 0	D 4	18/9	3	5/2	(CY2) = 0
	CZ	m	1 1	0 0 1 <B2> <B3>	1 0 0	C C	18/9	3	5/2	(Z) = 1
	CNZ	m	1 1	0 0 0 <B2> <B3>	1 0 0	C 4	18/9	3	5/2	(Z) = 0
	CP	m	1 1	1 1 0 <B2> <B3>	1 0 0	F 4	18/9	3	5/2	(S) = 0
	CM	m	1 1	1 1 1 <B2> <B3>	1 0 0	F C	18/9	3	5/2	(S) = 1
	CPE	m	1 1	1 0 1 <B2> <B3>	1 0 0	E C	18/9	3	5/2	(P) = 1
	CPO	m	1 1	1 0 0 <B2> <B3>	1 0 0	E 4	18/9	3	5/2	(P) = 0 If condition true, ((SP) − 1) ((SP) − 2) ← (PC) − 3 (PC) ← m (SP) ← (SP) − 2 If condition false, (PC) ← (PC) + 3
Return instruction	RET		1 1	0 1 1	0 0 1	C 9	10	1	3	(PC) ← ((SP) + 1) ((SP)), (SP) ← (SP) + 2
	RC		1 1	0 1 1	0 0 0	D 8	12/6	1	3/1	(CY2) = 1
	RNC		1 1	0 1 0	0 0 0	D 0	12/6	1	3/1	(CY2) = 0
	RZ		1 1	0 0 1	0 0 0	C 8	12/6	1	3/1	(Z) = 1
	RNZ		1 1	0 0 0	0 0 0	C 0	12/6	1	3/1	(Z) = 0
	RP		1 1	1 1 0	0 0 0	F 0	12/6	1	3/1	(S) = 0
	RM		1 1	1 1 1	0 0 0	F 8	12/6	1	3/1	(S) = 1
	RPE		1 1	1 0 1	0 0 0	E 8	12/6	1	3/1	(P) = 1
	RPO		1 1	1 0 0	0 0 0	E 0	12/6	1	3/1	(P) = 0 If condition true, (PC) ← ((SP) + 1) ((SP)), (SP) ← (SP) + 2 If condition false, (PC) ← (PC) + 1
Input/output control instruction	IN	n	1 1	0 1 1 <B2>	0 1 1	D B	10	2	3	(A) ← (Input buffer) (Input unit with device no. n)
	OUT	n	1 1	0 1 0 <B2>	0 1 1	D 3	10	2	3	(Output unit with device no. n) ← (A)
Interrupt control instruction	EI		1 1	1 1 1	0 1 1	F B	4	1	1	(INTE) ← 1
	DI		1 1	1 1 0	0 1 1	F 3	4	1	1	(INTE) ← 0
Stack operation instruction	PUSH	PSW	1 1	1 1 0	1 0 1	F 5	12	1	3	((SP) − 1) ← (A), ((SP) − 2) ← (F) (SP) ← (SP) − 2
	PUSH	B	1 1	0 0 0	1 0 1	C 5	12	1	3	((SP) − 1) ← (B), ((SP) − 2) ← (C) (SP) ← (SP) − 2
	PUSH	D	1 1	0 1 0	1 0 1	D 5	12	1	3	((SP) − 1) ← (D), ((SP) − 2) ← (E) (SP) ← (SP) − 2
	PUSH	H	1 1	1 0 0	1 0 1	E 5	12	1	3	((SP) − 1) ← (H), ((SP) − 2) ← (L) (SP) ← (SP) − 2
	POP	PSW	1 1	1 1 0	0 0 1	F 1	10	1	3	(F) ← ((SP)), (A) ← ((SP + 1) (SP) ← (SP) + 2
	POP	B	1 1	0 0 0	0 0 1	C 1	10	1	3	(C) ← ((SP)), (B) ← ((SP) + 1) (SP) ← (SP) + 2
	POP	D	1 1	0 1 0	0 0 1	D 1	10	1	3	(E) ← ((SP)), (D) ← ((SP) + 1) (SP) ← (SP) + 2
	POP	H	1 1	1 0 0	0 0 1	E 1	10	1	3	(L) ← ((SP)), (H) ← ((SP) + 1) (SP) ← (SP) + 2
Other	HLT		0 1	1 1 0	1 1 0	7 6	5	1	1	HALT status
	NOP		0 0	0 0 0	0 0 0	0 0	4	1	1	(PC) ← (PC) + 1
New instructions for 8085	RIM		0 0	1 0 0	0 0 0	2 0	4	1	1	Reads into accumulator all of the RST interrupt mask, pending RST interrupt request, and serial input data at SID pin.
	SIM		0 0	1 1 0	0 0 0	3 0	4	1	1	Masks corresponding RST interrupt with accumulator value (bit pattern). Enables serial output so as to load output bits into SOD latch.

<table>
<tr><th>Symbol</th><th>Contents</th></tr>
<tr><td>r</td><td>Represents register</td></tr>
<tr><td>m</td><td>2-byte data</td></tr>
<tr><td>n</td><td>1-byte data</td></tr>
<tr><td><B2></td><td>2nd byte of instruction</td></tr>
<tr><td><B3></td><td>3rd byte of instruction</td></tr>
<tr><td>AAA</td><td>Binary equivalent of n in RST instructions</td></tr>
<tr><td>F</td><td>Eight-bit data including flags such as S, Z, P, CY1 and CY2. These flags are configured in the order of S, Z, X, CY1, X, P, X and CY2; where X shows undetermined flag.</td></tr>
<tr><td>PC</td><td>Program counter</td></tr>
<tr><td>SP</td><td>Stack pointer</td></tr>
<tr><td>SSS
or
DDD</td><td>Sequential order determined by register or storage contents.
Table shown below lists order values for SSS or DDD,

where
M = (H) (L)
<table>
<tr><th>Register or storage</th><th>S S S or D D D</th></tr>
<tr><td>B</td><td>0 0 0</td></tr>
<tr><td>C</td><td>0 0 1</td></tr>
<tr><td>D</td><td>0 1 0</td></tr>
<tr><td>E</td><td>0 1 1</td></tr>
<tr><td>H</td><td>1 0 0</td></tr>
<tr><td>L</td><td>1 0 1</td></tr>
<tr><td>M</td><td>1 1 0</td></tr>
<tr><td>A</td><td>1 1 1</td></tr>
</table></td></tr>
<tr><td>←</td><td>Indicates direction of data trasfer</td></tr>
<tr><td>( )</td><td>Indicates contents of register, storage, etc.</td></tr>
<tr><td>∨</td><td>Logical sum</td></tr>
<tr><td>∀</td><td>Exclusive logical sum</td></tr>
<tr><td>∧</td><td>Logical product</td></tr>
<tr><td>−</td><td>Negate</td></tr>
</table>

Note: The number of states and cycles shown above also show satisfied and unsatisfied conditions.

Electrical Characteristics

- Absolute maximum ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	Vcc	Reference to GND	−0.5 ~ +7	V
Input voltage	V_{IN}		−0.5 ~ Vcc +0.5	V
Output voltage	V_{OUT}		−0.5 ~ Vcc +0.5	V
Storage temperature	Tstg	Ta = 25°C	−55 ~ +150	°C
Allowable power dissipation	P_D	Ta = 25°C	1.0	W

- Operating range

Parameter	Symbol	Conditions	Unit
Supply voltage	Vcc	3 ~ 6	V
Operating temperature	Top	−40 ~ +85	°C

- Recommended operating conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage	Vcc	4.5	5	5.5	V
Operating temperature	Top	−40	+25	+85	°C
Low input voltage level	V_{IL}	−0.3		+0.8	V
High input voltage level	V_{IH}	2.2		Vcc +0.3	V

- Static electrical characteristics

Parameter	Symbol	Measurement conditions		MIN	TYP	MAX	Unit
Low output voltage level	V_{OL}	I_{OL} = 2 mA	Vcc = 4.5 V ~ 5.5 V Ta = −40 °C ~ +85 °C			0.45	V
High output voltage level	V_{OH}	I_{OH} = −400μA		2.4			V
		I_{OH} = −40μA		4.2			V
Input leakage current	I_{LI}	0≤V_{IN}≤Vcc		−10		10	μA
Output leakage current	I_{LO}	0≤V_{OUT}≤Vcc		−10		10	μA
Supply current	Icc	Tcyc = 320 ns CL = 0 Reset signal applied			11	22	mA
			Vcc = 4.75 V ~ 5.25 V Ta = 0 °C ~ +85 °C		11	17	mA

- Switching characteristics

(Ta = −40°C ~ 85°C, Vcc = 4.5 V ~ 5.5 V)

Parameter	Symbol	Measurement conditions	MIN	MAX	Unit
Clock period	t_{CYC}		320	2000	ns
Low-level time lapse for clock	t_1	t_{CYC} = 320 ns	80		ns
High-level time lapse for clock	t_2	CL = 150 pF	120		ns
Clock rise or fall time	t_r, t_f			30	ns
Delay time from leading edge of X1 to that of CLK	t_{XKR}		30	120	ns
Delay time from leading edge of X1 to trailing edge of CLK	t_{XKF}		30	150	ns
Delay time (1) from A8–15 valid to trailing edge of ALE	t_{AC}		270		ns
Delay time from A0–7 valid to trailing edge of control signal	t_{ACL}		240		ns
Time from A0–15 valid to data input	t_{AD}			575	ns
Time from trailing edge of $\overline{RD}$ ($\overline{INTA}$) from address floating state	t_{AFR}			0	ns
Delay time (1) from A8–15 valid to trailing edge of ALE	t_{AL}		115		ns
Delay time from A0–7 valid to trailing edge of ALE	t_{ALL}		90		ns
Time from address valid to READY status	t_{ARY}			220	ns
Time for which address is determined after leading edge of control signal	t_{CA}		120		ns
Control signal pulse width	t_{CC}		400		ns
Delay time from leading edge of control signal to that of ALE	t_{CL}		40		ns
Data set-up time for leading edge of $\overline{WR}$	t_{DW}		420		ns
Delay time from trailing edge of HLDA to activated state	t_{HABE}			210	ns
Delay time from leading edge of HLDA to bus floating state	t_{HABF}			210	ns
Time from HLDA valid to leading edge of CLK	t_{HACK}		110		ns

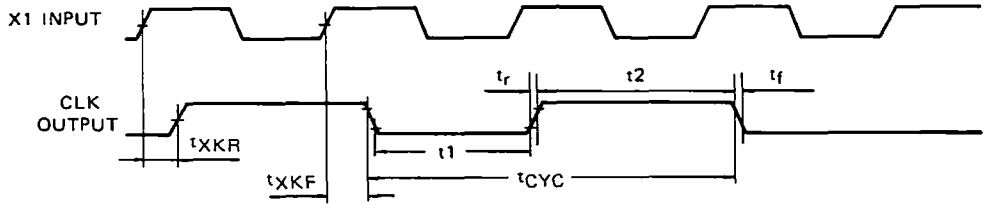
Parameter	Symbol	Measurement conditions	MIN	MAX	Unit
Hold time of HOLD for trailing edge of CLK	t_{HDH}	t_{CYC} = 320 ns CL = 150 pF	0		ns
Set-up time of HOLD for trailing edge of CLK	t_{HDS}		170		ns
Hold time of INTR for trailing edge of CLK	t_{INH}		0		ns
Set-up time of INTR for trailing edge of CLK	t_{INS}		160		ns
Time for which address is valid after trailing edge of ALE	t_{LA}		100		ns
Delay time from trailing edge of ALE to trailing edge of control signal	t_{LC}		130		ns
Time from trailing edge of ALE to that of CLK	t_{LCK}		100		ns
Time from trailing edge of ALE to valid data at read	t_{LDR}			460	ns
Time from trailing edge of ALE to valid data at write	t_{LDW}			200	ns
ALE signal pulse width	t_{LL}		140		ns
Time for setting READY against trailing edge of ALE	t_{LRY}			110	ns
Delay time from leading edge of $\overline{RD}$ to determination of next address	t_{RAE}		150		ns
Time from trailing edge of $\overline{RD}$ ($\overline{INTR}$) to valid data	t_{RD}			300	ns
Time from leading edge of control signal to trailing edge of control signal	t_{RV}		400		ns
Data hold time for leading edge of $\overline{RD}$ ($\overline{INTA}$)	t_{RDH}		0		ns
Hold time of READY for leading edge of CLK	t_{RYH}		0		ns
Set-up time of READY for leading edge of CLK	t_{RYS}		110		ns
Time for valid data after leading edge of $\overline{WR}$	t_{WD}		100		ns

Parameter	Symbol	Measurement conditions	MIN	MAX	Unit
Delay time from trailing edge of $\overline{WR}$ to data validity	tWDL	tCYC = 320 ns CL = 150 pF		40	ns

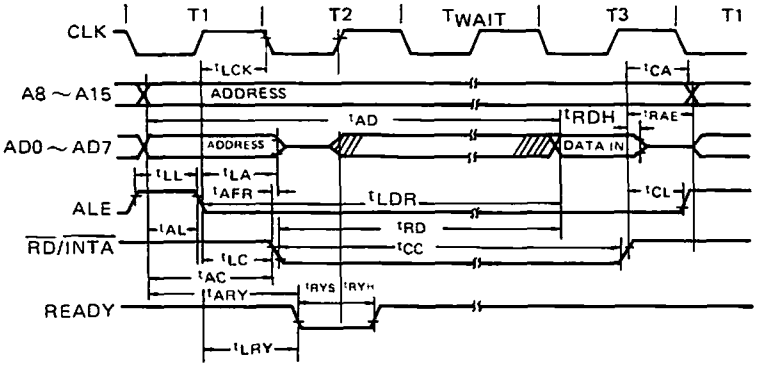
Notes:
1. The specifications for A8 through A15 apply to IO/$\overline{M}$, S0, and S1 except that T4 through T6 are undefined.
2. Timings are all measured on condition that V_{OL} = 0.8 V, V_{OH} = 2.2 V, and input reference voltage is 1.5 V.

Timing Charts

- Clock waveform

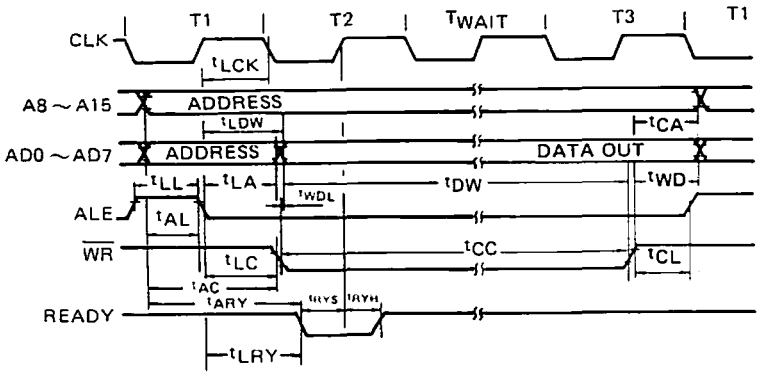


- Read cycle



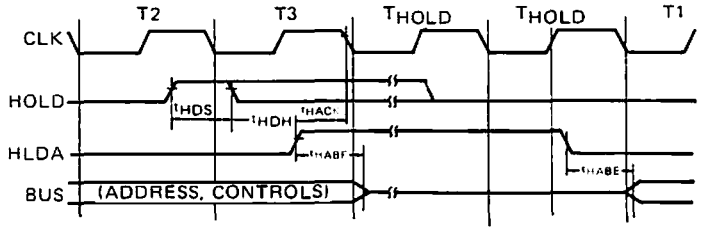
Note: READY must stay unchanged throughout set-up and hold times.

- Write cycle

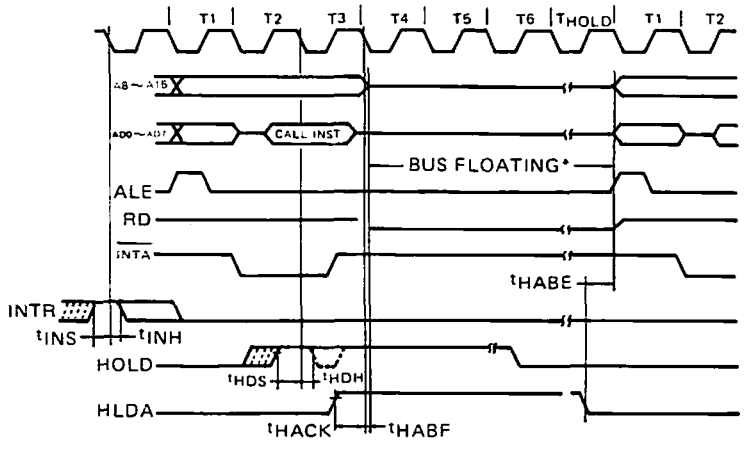


Note: READY must stay unchanged throughout set-up and hold times.

- Hold cycle



- Interrupt and hold cycle



*: During this time lapse, IO/$\overline{M}$ is floating.

MSM81C55RS/GS

2048-Bit CMOS Static RAM with I/O Ports and Timer

General

The MSM81C55RS is a static RAM in combination with I/O ports and timer, for use with microprocessors. The MSM81C55RS is made from silicon-gate CMOS technology. It features very low power dissipation of up to 100 μA as standby current when not selected.

The MSM81C55 has 2K-bit of static RAM, configured as 256 x 8 bits. The MSM81C55RS has an access time of 400 ns at maximum so that it can be used also in the 80C85A system without wait states.

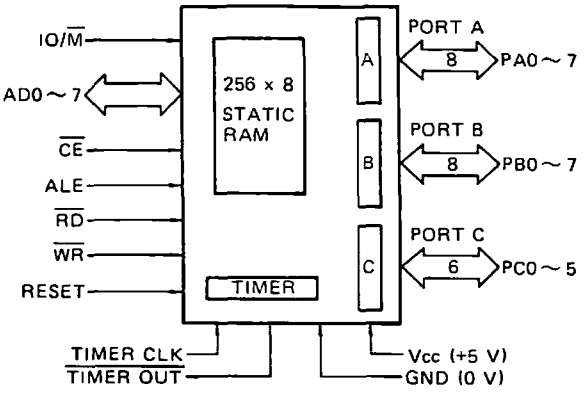
The MSM81C55RS has three general purpose I/O ports: two 8-bit ports and one 6-bit port, respectively, ports A, B, and C. Port C is used to enable and set the modes for the other two ports.

MSM81C55RS also has a 14-bit built-in programmable counter/timer which can be used to generate square pulses for timers or count pulses.

Features

- High-speed operation and low power dissipation
- RAM configuration of 256 x 8-bit bytes
- Single power supply of 3 V to 6 V
- Completely static operation
- Built-in address latch circuitry
- 8-bit programmable I/O ports (ports A and B)
- 6-bit programmable I/O port (port C)
- 14-bit programmable binary counter/timer
- Multiplexed address/data buses
- 40-pin DIP (MSM81C55RS)
- 44-pin flat package (MSM81C55GS)
- Compatible with Intel 8155

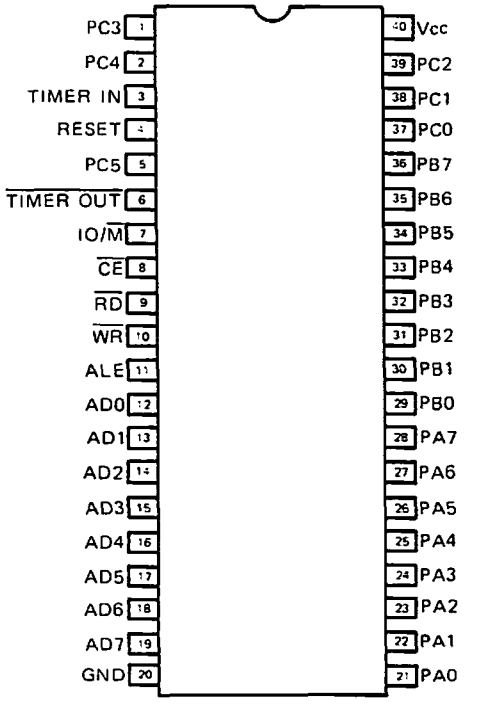
Circuit Configuration



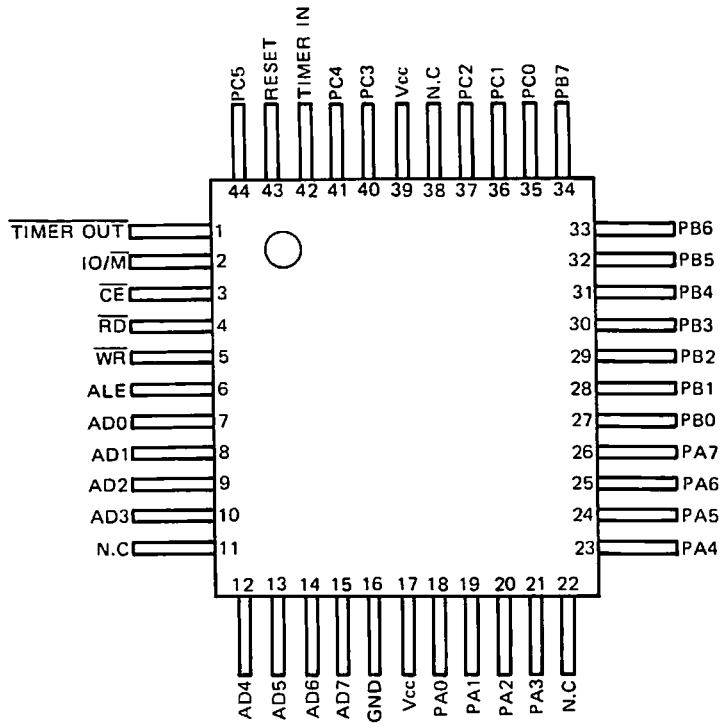
(These specifications are subject to change without notice.)

Pin Connections

MSM81C55RS (Top View) 40 Lead Plastic DIP



MSM81C55GS (Top View) 44 Lead Plastic Flat Package



*: Model names on products may be abbreviated.

Electrical Characteristics

- Absolute maximum ratings

Parameter	Symbol	Conditions	Ratings		Unit
			MSM81C55RS	MSM81C55GS	
Supply voltage	Vcc	In reference to GND	−0.5 ~ +7		V
Input voltage	VIN		−0.5 ~ Vcc +0.5		V
Output voltage	VOUT		−0.5 ~ Vcc +0.5		V
Storage temperature	Tstg	Ta = 25°C	−55 ~ +150		°C
Allowable power dissipation	PD	Ta = 25°C	1.0	0.7	W

- Operating range

Parameter	Symbol	Ratings	Unit
Supply voltage	Vcc	3 ~ 6	V
Operating temperature	TOP	−40 ~ +85	°C

- Recommended operating conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage	Vcc	4.5	5	5.5	V
Operating temperature	TOP	−40	+25	+85	°C
Low input voltage level	VIL	−0.3		+0.8	V
High input voltage level	VIH	2.2		Vcc +0.3	V

- Static electrical characteristics

Parameter	Symbol			MIN	TYP	MAX	Unit
Low output voltage level	VOL	IOL = 2 mA	Vcc = 4.5 V ~ 5.5 V Ta = −40°C ~ +85°C	−	−	0.45	V
High output voltage level	VOH	IOH = −400μA		2.4	−	−	V
		IOH = −40μA		4.2	−	−	V
Input leakage current	ILI	0≦VIN≦Vcc		−10	−	10	μA
Output leakage current	ILO	0≦VOUT≦Vcc		−10		10	μA
Standby supply current	Iccs	CE≧Vcc − 0.2 V VIH≧Vcc − 0.2 V VIL≦0.2 V		−	0.1	100	μA
Average operating supply current	Icc	Storage cycle time: 1 μs		−	−	5	mA

- Switching characteristics

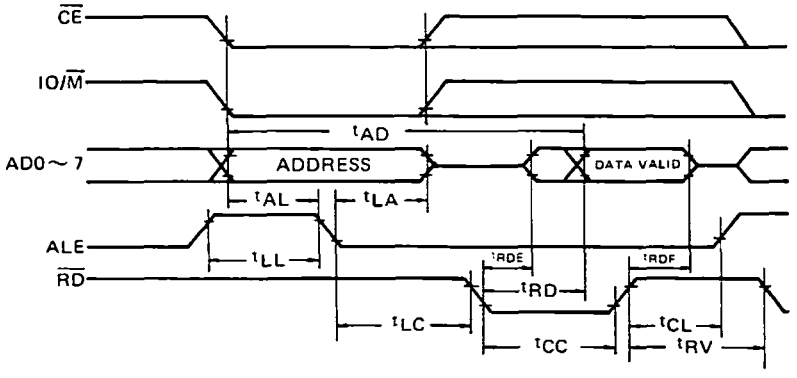
(Vcc = 4.5 V ~ 5.5V, Ta = −40 ~ +85°C)

Parameter	Symbol	MIN	MAX	Unit	Remarks
Address-to-Latch Set Time	t_{AL}	50		ns	C_L = 150 pF
Latch-to-Address Hold Time	t_{LA}	30		ns	
Latch-to-Read (Write) Delay Time	t_{LC}	100		ns	
Read-to-Output Delay Time	t_{RD}		170	ns	
Address-to-Output Delay Time	t_{AD}		400	ns	
Latch Width	t_{LL}	100		ns	
Read-to-Data Bus Float Time	t_{RDF}	0	100	ns	
Read (Write)-to-Latch Delay Time	t_{CL}	20		ns	
Read (Write) Width	t_{CC}	250		ns	
Data-to-Write-set Time	t_{DW}	150		ns	
Write-to-Data-in Hold Time	t_{WD}	0		ns	
Recovery Time	t_{RV}	300		ns	
Write-to-Port Output Delay Time	t_{WP}		400	ns	
Port Input-to-Read Set Time	t_{PR}	70		ns	
Read-to-Port Input Hold Time	t_{RP}	50		ns	
Storbe-to-Buffer Full Delay Time	t_{SBF}		400	ns	
Strobe Width	t_{SS}	200		ns	
Read-to-Buffer Empty Delay Time	t_{RBE}		400	ns	
Strobe-to-Interrupt ON Delay Time	t_{SI}		400	ns	
Read-to-Interrupt OFF Delay Time	t_{RDI}		400	ns	
Port Input-to-Strobe Set Time	t_{PSS}	50		ns	
Strobe-to-Port Input Hold Time	t_{PHS}	120		ns	
Strobe-to-Buffer Empty Delay Time	t_{SBE}		400	ns	
Write-to-Buffer Full Delay Time	t_{WBF}		400	ns	
Write-to-Interrrpt OFF Delay Time	t_{WI}		400	ns	
Timer Output Delay Time (Low Level)	t_{TL}		400	ns	
Timer Output Delay Time (High Level)	t_{TH}		400	ns	
Read-to-Data Bus Enable Delay Time	t_{RDE}	10		ns	
Timer Cycle Time	t_{CYC}	320		ns	
Timer Input Rise/Fall Time	t_r, rf		80	ns	
Timer Input Low Level Time	t1	80		ns	
Timer Input High Level Time	t2	120		ns	

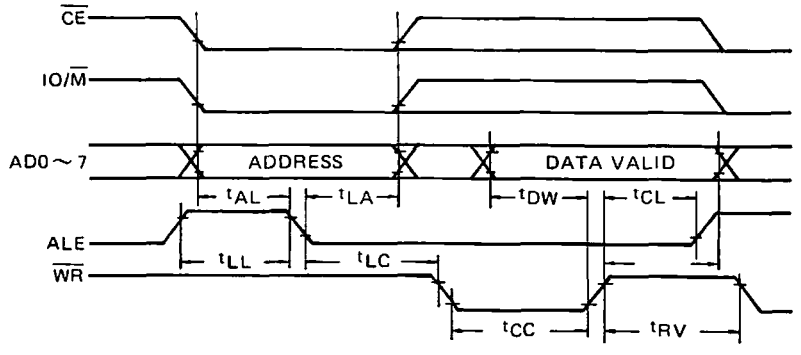
Note: The above timings for both input and output are all measured with V_L = 0.8 V and V_H = 2.2 V as the reference level.

Timing Charts

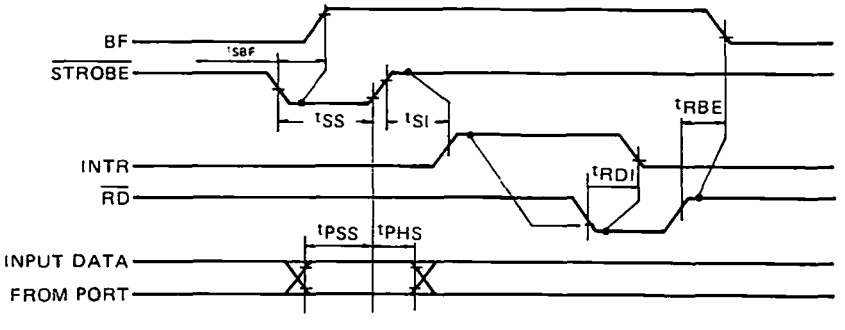
- Read cycle



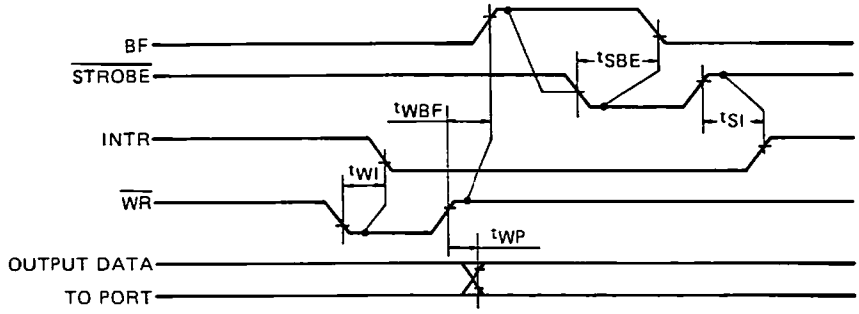
- Write cycle



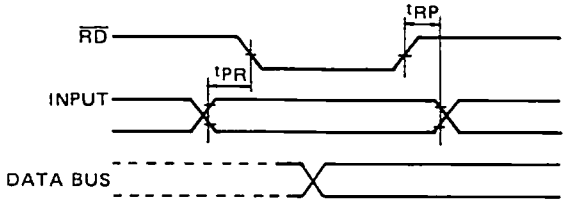
- Strobed input mode



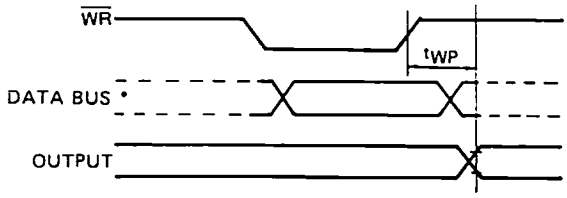
- Strobed output mode



- Basic input mode

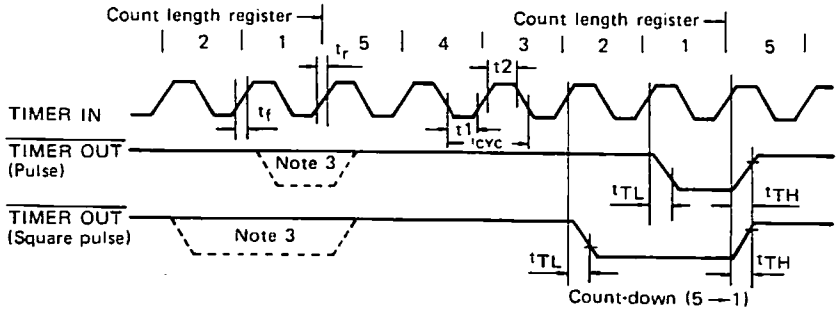


- Basic output mode



*The timing for DATA BUS is the same as that for read or write cycle.

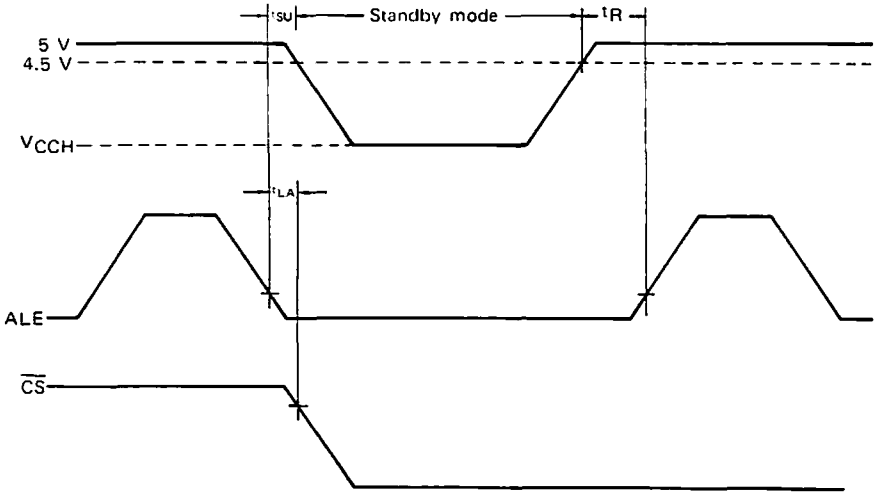
- Timer waveform



Note 3: This dotted-line pulse is periodically output depending on the program contents for the output mode (M1 = 1).

RAM Data Holding Characteristics on Low Supply Voltage

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Data Holding Supply Voltage	V_{CCH}	V_{IN} = 0 V or Vcc, ALE = 0 V	2.0	–	–	V
Data Holding Supply Current	I_{CCH}	Vcc = 2 V, ALE = 0 V_{IN} = 0 V or Vcc	–	0.05	2.0	μA
Set-Up Time	t_{SU}		30	–	–	ns
Hold Time	t_R		20	–	–	ns

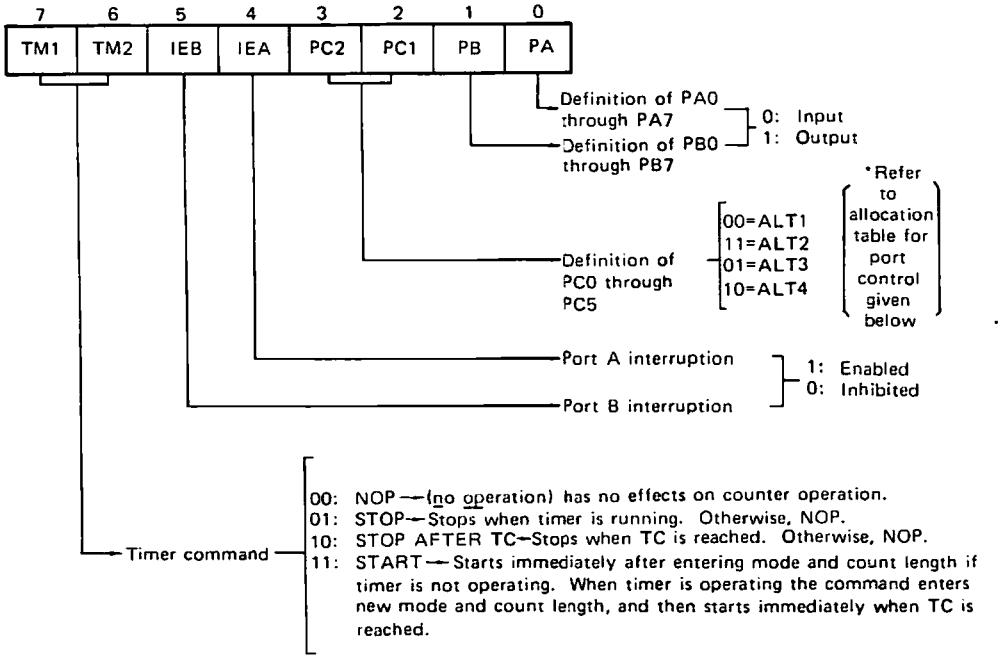


Description of Pins Functions

Pin Symbol	Functions
RESET	A high level at this pin resets the system, and forces the three I/O ports to input mode.
ALE	At the trailing edge of ALE (address latch enable), AD0 to AD7, IO/$\overline{M}$, and $\overline{CE}$ are latched.
AD0 ~ 7	Tri-state bilateral address/data buses. These buses latch 8-bit address data at the trailing edge of ALE. They are used for 8-bit data transfers with direction determined by $\overline{WRITE}$ or $\overline{READ}$.
$\overline{CE}$	A high level at $\overline{CE}$ inhibits both read and write.
IO/$\overline{M}$	A high level at IO/$\overline{M}$ signal selects IO, a low level selects RAM memory.
$\overline{RD}$	A low level at $\overline{RD}$ enables a read from RAM onto AD0 to AD7 during a RAM cycle or selected port data durnig an I/O cycle.
$\overline{WR}$	A low level at $\overline{WR}$ enables data on AD0 to AD7 to be written to RAM during a RAM cycle or to a selected port during an I/O cycle.
PA0 ~ 7 (PB0 ~ 7)	General-purpose I/O pins. The direction of data is determined by programming the command/status register (C/S register).
PC0 ~ 7	Can be used as a general purpose I/O pin or control pin for PA or PB port. Functions of these pins when used as control terminals are: PC0 . . . A INTR (Port A interrupt) PC1 . . . A BF (Port A buffer full) PC2 . . . $\overline{A\ STB}$ (Port A strobe) PC3 . . . A INTR (Port B interrupt) PC4 . . . B BF (Port B buffer full) PC5 . . . $\overline{B\ STB}$ (Port B strobe)
TIMER IN	Input signal for counter/timer
$\overline{TIMER\ OUT}$	Timer output signal. This pin outputs square pulses and other pulses depending on internal programming.
Vcc	Power supply of +5 V
GND	GND

Description for Operations

(1) Programming command/status (C/S) register
The command register is an 8-bit latch. The C/S register contents can be changed anytime by writing to IO address XXXXX000 in an IO cycle. The bit configuration for the C/S register is shown below.

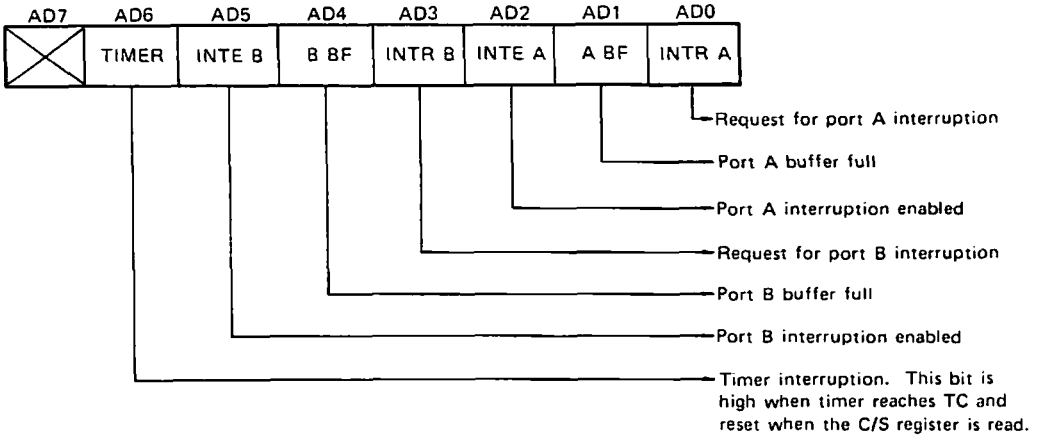


*Allocation table for port control

	ALT1	ALT2	ALT3	ALT4
PC0	Input port	Output port	A INTR	A INTR
PC1	Input port	Output port	A BF	A BF
PC2	Input port	Output port	$\overline{\text{A STB}}$	$\overline{\text{A STB}}$
PC3	Input port	Output port	Output port	B INTR
PC4	Input port	Output port	Output port	B BF
PC5	Input port	Output port	Output port	$\overline{\text{B STB}}$

(2) Read C/S register

The status register is a 7-bit latch and holds I/O and timer status. The C/S register is read at IO address XXXXX000. Configuration of the status word is shown below.



(3) PA, PB registers

Both registers can be used as either input or output ports according to programming of the C/S register. They can also be used in the basic or strobe mode. The IO address of the PA register is XXXXX001; that of the PB register is XXXXX010.

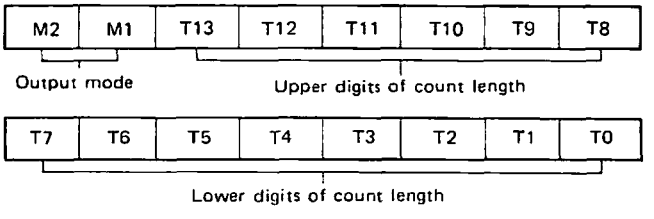
(4) PC register

The PC register can be used as an input port, output, or for control signal according to the contents of C/S register. IO address of the PC register is XXXXX011.

(5) Timer

This is a 14-bit counter which counts TIMER pulses and outputs a square pulse when the final value of TC is reached. The IO address of the timer register's lower byte is XXXXX100. While that of its upper byte is XXXXX101.

The timer can be programmed, byte by byte, by writing to the count length register (CLR) while selecting the timer address during a write. Bits 0 to 13 store the count length and bits 14 and 15 the timer output mode. The operator can read the counter contents and the output mode. The initial value is first to the counter register. It can be take any value from 2 through 3FFF (hexadecimal). Timer format and output mode are shown below.



M2	M1	
0	0	Low level is output during the latter half (Note 1) of the counting period.
0	1	Low level is output during the latter half of the counting period; and a count length automatically programmed is entered when the final value TC is reached. Then the operation is repeated.
1	0	A pulse is output when the final value TC is reached.
1	1	A pulse is output each time the final value TC is reached; automatically inputting a count length which has been given in the program. Then the operation is repeated.

Note 1: In the case of an asymmetric count, such as 9, the output is high for 5 counts, and low for four.

Note 2: When the MSM81C55RS is reset, it stops counting. The counter is not set to any specific initial value or output mode. To resume counting after a reset, use the START instruction in the C/S register.

(6) Standby mode

Standby mode is provided at the trailing edge of ALE after $\overline{CE}$ is disasserted. This is because $\overline{CE}$ from the MSM81C55RS is latched at the leading edge of ALE. Simultaneously the levels of the input port and timer input should be set at a potential of Vcc or GND. A battery should be used only after setting the level of output ports low or using all ports as input ports, and also setting the timer output to low or adding a buffer whose power-supply terminal is connected to the battery.